

# Ravi Hosabettu

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## Objective

A position as a research and development engineer in applying formal methods to validate system designs and in developing new verification methodologies.

## Research interests

- Formal verification of pipelined microprocessors.
- Combining theorem proving and model checking for large state-of-the-art design verification.
- Formal verification of memory models and cache coherency.

## Education

Doctoral student since Fall 1995, University of Utah, Salt Lake City

Major: Computer Science, GPA: 3.98/4.00

Dissertation Title: *Systematic Verification of Pipelined Microprocessors*

Advisor: Dr. Ganesh Gopalakrishnan

**Ph.D.** expected in February 2000

Awarded *University of Utah Graduate Research Fellowship* for the academic year 1999-2000.

**Master of Technology**, February 1994, Indian Institute of Technology, Kanpur, India

Major: Computer Science, CPI: 10.00/10.00

Thesis: *On the Centerpoint Problem in Computational Geometry*

**Bachelor of Technology**, June 1992, Karnataka Regional Engineering College, India

Major: Computer Engineering, Marks: 85.5%

Senior Project: *Implementation of a File Transfer Protocol*

Received merit scholarship throughout the program and stood third in the entire university.

## Work experience

- Student Associate at SRI International (Stanford Research Institute) during Summer 1997 and Summer 1998. During this period, I worked on a technique for pipelined processor verification and on developing an efficient decision procedure for bit-vector theory.
- Research Assistant in the department of Computer Science, University of Utah under Dr. Ganesh Gopalakrishnan—Summer 1996 to Spring 1997, Fall 1997 to Spring 1998 and Fall 1998 to Summer 1999.

- Teaching Assistant in the department of Computer Science, University of Utah from Fall 1995 to Spring 1996.
- Senior Engineer at Wipro Infotech, Ltd. India for 18 months from March 1994 to August 1995. During this period:

I was part of a group that wrote device drivers for Novell, Inc for their OS Unixware. Specifically, I wrote a device driver for arbitrating access to the parallel port while multiple devices such as printer, trakker were connected to the parallel port. Our group was awarded the 'best project award' for 1994.

I was the project leader for the group that wrote device drivers/firmware for Wipro's own PCI-RAID controller. Specifically, I wrote the firmware and did the managing work.

- Teaching Assistant in the department of Computer Science, Indian Institute of Technology, Kanpur for 1 year, July 1992 - June 1993.

## Publications

1. Ravi Hosabettu, Ganesh Gopalakrishnan and Mandayam Srivas. *A Proof of Correctness of a Processor Implementing Tomasulo's Algorithm Without a Reorder Buffer*. Tenth IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, Bad Herrenalb, Germany, September 1999.
2. Ravi Hosabettu, Mandayam Srivas and Ganesh Gopalakrishnan. *Proof of Correctness of a Processor with Reorder Buffer using the Completion Functions Approach*. Eleventh International Conference on Computer Aided Verification, Trento, Italy, July 1999.
3. Ravi Hosabettu, Mandayam Srivas and Ganesh Gopalakrishnan. *Decomposing the Proof of Correctness of Pipelined Microprocessors*. Tenth International Conference on Computer Aided Verification, BC, Canada, 1998.
4. Abdel Mokkedem, Ravi Hosabettu and Ganesh Gopalakrishnan. *Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem*. Second International Conference on Formal Methods in Computer-Aided Design, Palo Alto, USA, 1998.
  - An extended version accepted for publication in a special issue of the journal Formal Methods in System Design.
5. Ganesh Gopalakrishnan, Rajnish Ghughal, Ravi Hosabettu, Abdelillah Mokkedem and Ratan Nalumasu. *Formal Modeling and Validation Applied to a Commercial Coherent Bus: A Case Study*. Ninth IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods, Montreal, Canada, 1997.
6. Ravi M Hosabettu and Asish Mukhopadhyay. *Computing a Weighted Centerpoint of a Special Configuration of Points in Linear Time*. Seventh SIAM Conference on Discrete Mathematics, Albuquerque, New Mexico, 1994.
7. Asish Mukhopadhyay, Alok Aggarwal, Ravi Hosabettu. *On the Ordinary Line Problem in Computational Geometry*. Fourth National Seminar on Theoretical Computer Science, IIT Kanpur, India, 1994.
  - An extended version of the paper appears in the Nordic Journal of Computing, Volume 4, Winter 1997.

## Presentations

1. On “A Proof of Correctness of a Processor Implementing Tomasulo’s Algorithm Without a Reorder Buffer” at the Conference on Correct Hardware Design and Verification Methods, Germany, September 1999.
2. On “Proof of Correctness of a Processor with Reorder Buffer using the Completion Functions Approach” at the Conference on Computer Aided Verification, Italy, July 1999.
3. On “Decomposing the Proof of Correctness of Pipelined Microprocessors” at the Conference on Computer Aided Verification, Canada, June 1998.

## Refereeing

1. Conference on Formal Methods in Computer-Aided Design, 1998; Conference on Correct Hardware Design and Verification Methods, 1999; International Conference on Computer Design, 1999.
2. Helped Dr. Ganesh Gopalakrishnan evaluate one Ph.D. thesis and many other papers.

## Verification formalisms and tools

- *Formalisms:* Temporal Logic,  $\omega$ -automata, First Order Logic and Rewriting.
- *Tools:* PVS, SMV, SPIN, SVC, MDG-tools, VIS and ACL2

## Course work

Formal Methods in System Design	Automated Deduction	VLSI Architectures
Next Generation Architectures	Adv. Computer Organization	Digital System Design
Programming Linguistics	Functional Programming	Nonmonotonic Reasoning
Analysis of Algorithms	Parallel Graph Algorithms	Complexity Theory
Computer Aided Geometric Design	Computer Graphics	Computational Geometry
Data Communication Networks	Operating Systems	Database Systems

## Languages and computer skills

- **Languages:** Pascal, C, C++, VHDL, ML, Scheme, Lisp, Prolog, Fortran.
- **Operating Systems:** Unix, Linux, Windows-NT, Netware, MS-DOS.
- **Graphics Tools:** Tcl/Tk, Postscript.

## Miscellaneous

- Availability: March 1, 2000.
- References: Available upon request.

# Dissertation

**Defense:** In February 2000.

**Title:** *Systematic Verification of Pipelined Microprocessors*

**Abstract:** We propose a systematic approach called the *Completion Functions Approach* to decompose and incrementally build the proof of correctness of pipelined microprocessors. The central idea is to construct the abstraction function using completion functions, one per unfinished instruction, each of which specifies the effect on the observables of completing the instruction. This construction of the abstraction function leads to a very natural decomposition of the proof. The approach does not involve the construction of an explicit intermediate abstraction, supports incremental verification facilitating debugging and error localization, and is applicable uniformly on a wide variety of pipelined processor designs.

The methodology is implemented in PVS and it makes heavy use of strategies based on decision procedures and rewriting to automate significant portions of the proof. It has been applied to many example processor designs with reasonable manual effort. The latest design verified is an example out-of-order execution processor with a reorder buffer, a load-store buffer, branch prediction, speculative execution and exceptions. The verification was completed in 35 person days.