

STRIDE- AND GLOBAL HISTORY- BASED DRAM PAGE MANAGEMENT

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MOTIVATION

Speculative Precharge and Activate

Use Prefetching techniques for speculation

OVERVIEW

Motivation

Scheduler

Memory Requirements

Experimental Results

Questions

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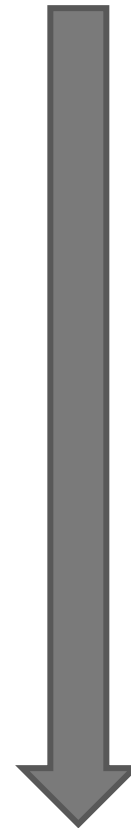
SCHEDULER

Three components:

BASE SCHEDULER

**CONSTANT STRIDE
DETECTING OPEN/CLOSE
PAGE PREDICTOR**

**GLOBAL HISTORY- BASED
CLOSE PAGE PREDICTOR**



**COMMAND
ISSUING
PRIORITY**

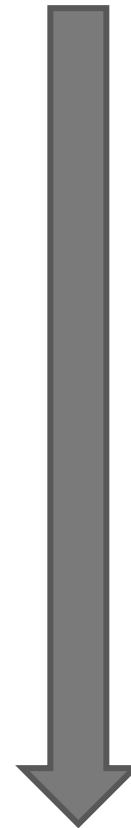
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BASE SCHEDULER

Read and Write requests served in bursts

- BUS switching delay

WRITE DRAIN

MODE:

WRITE QUEUE LENGTH > 40

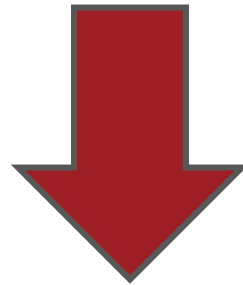
Until

WRITE QUEUE LENGTH < 20

READ MODE:

WRITE DRAIN MODE

FR-FCFS (write queue)



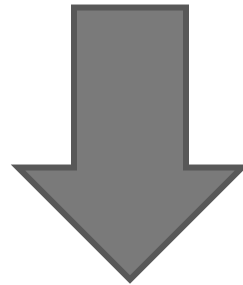
IF NONE
ISSUABLE

PRE or ACT cmd
from read queue

*NO BANK CONFLICT WITH
PENDINGWRITE REQUESTS*

READ MODE

FR-FCFS (read queue)



IF NONE
ISSUABLE

PRE from write
queue

*NO BANK CONFLICT WITH
PENDING READ REQUESTS*

ISUSED DATA STRUCTURE

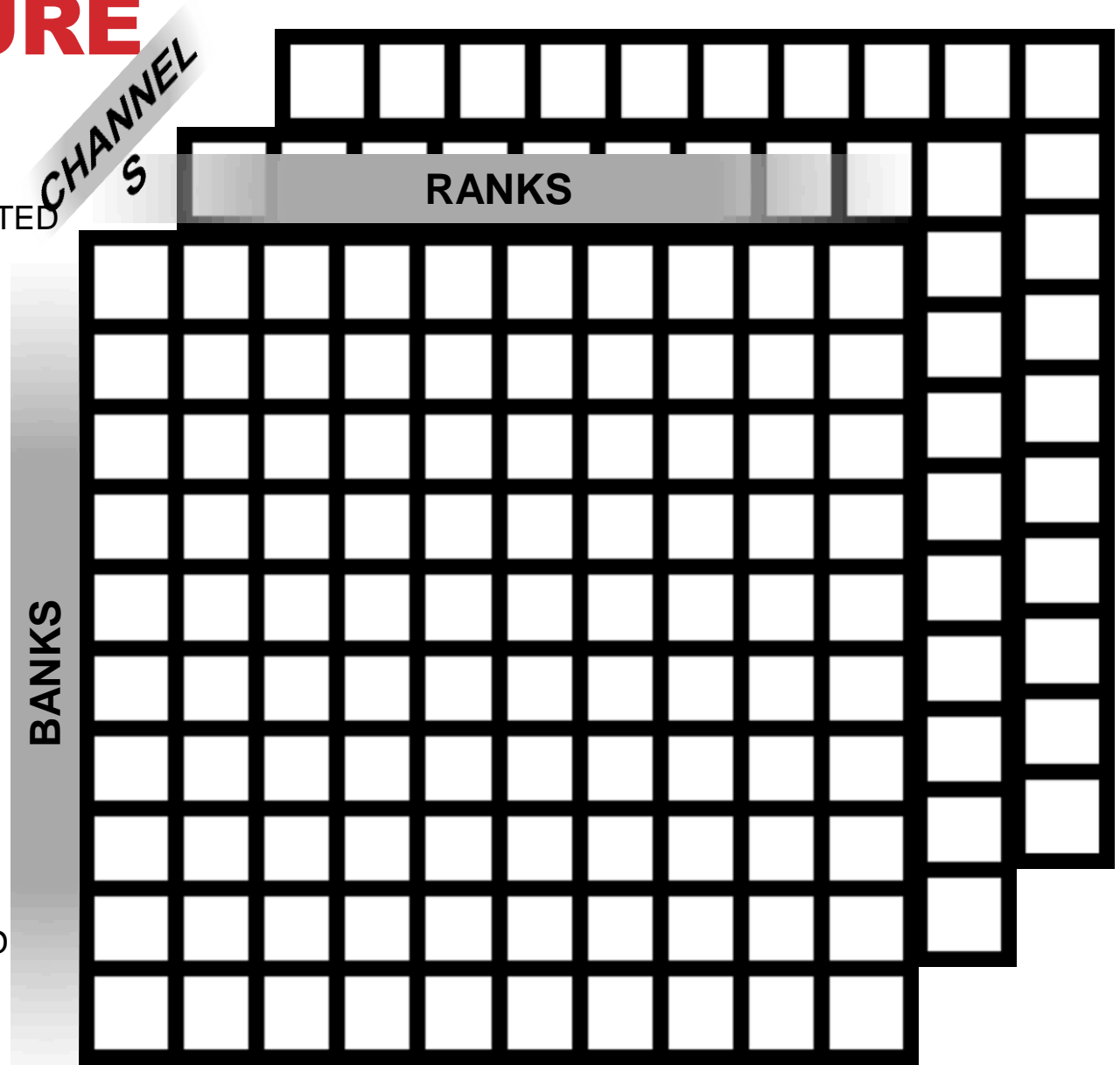
VALUES:

0: BANK NOT TARGETTED BY ANY REQUEST

1: BANK TARGETTED BY ATLEAST ONE READ REQUEST

2: BANK TARGETTED BY ATLEAST ONE WRITE REQUEST

3: BANK TARGETTED BY ATLEAST ONE WRITE & ONE READ REQUEST



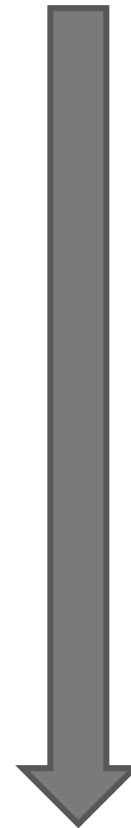
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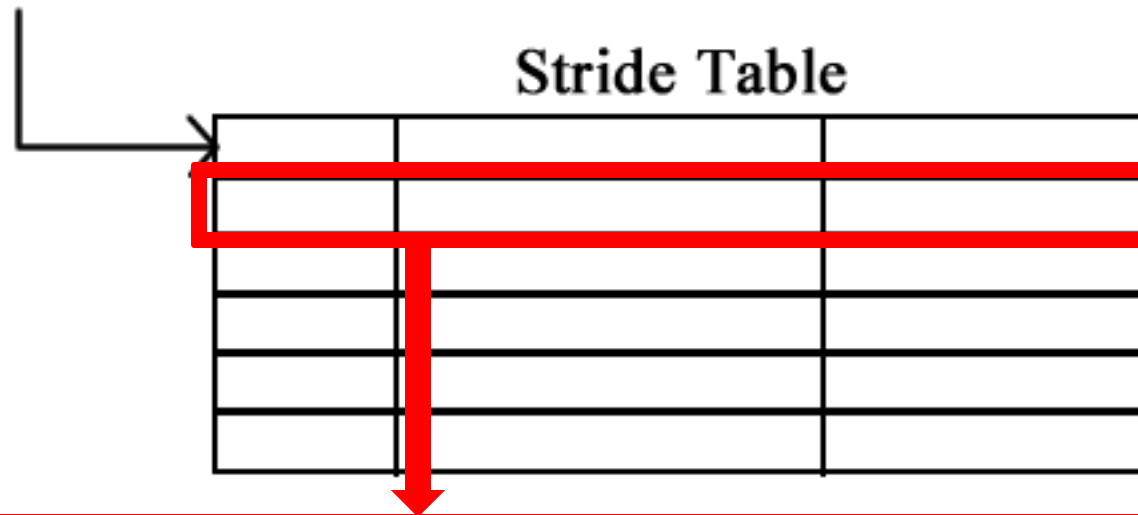
**GLOBAL HISTORY- BASED
CLOSE PAGE PREDICTOR**



**COMMAND
ISSUING
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CONSTANT STRIDE DETECTING OPEN/CLOSE PAGE PREDICTOR

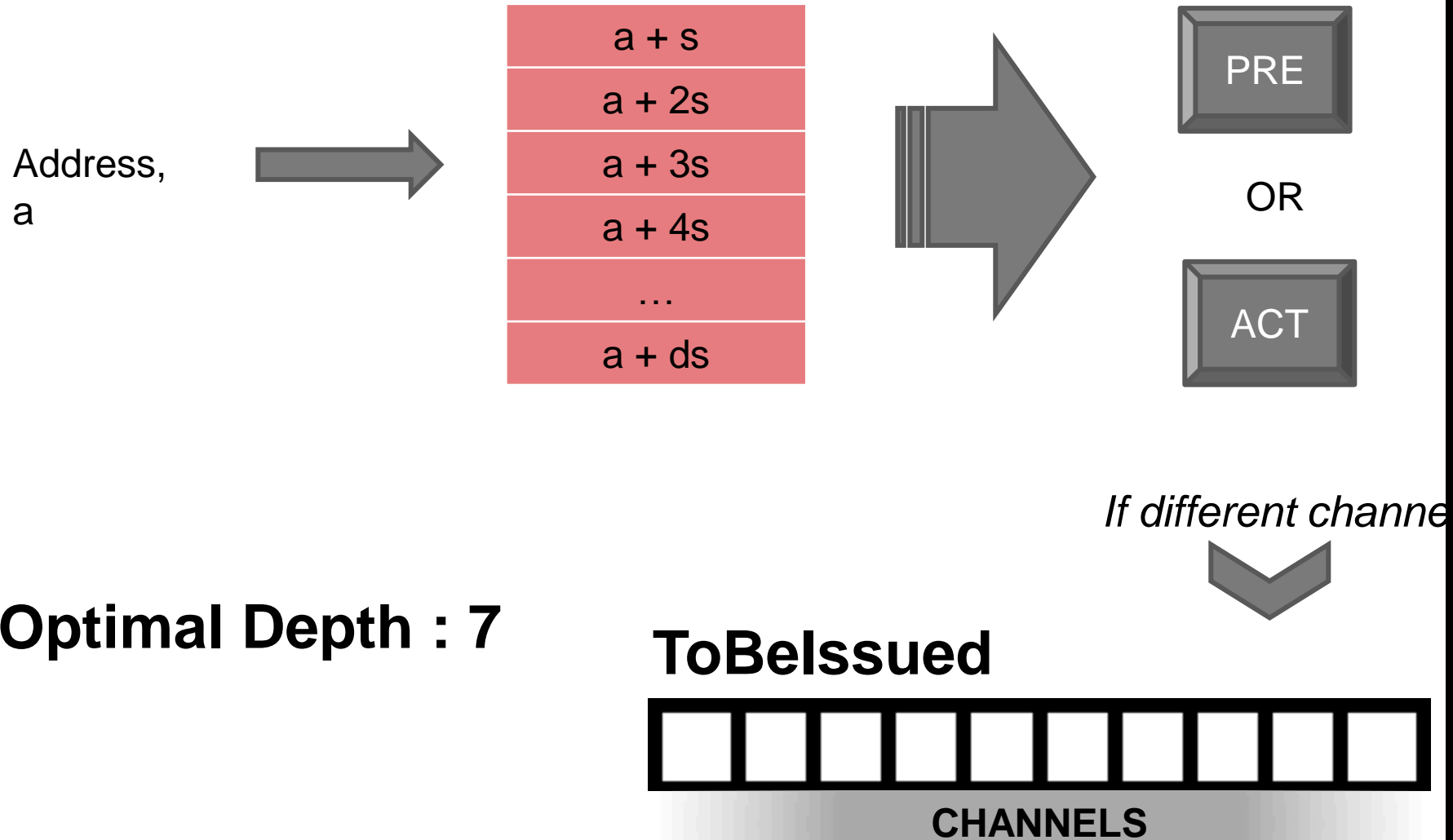
Instruction PC % 1024



**DETECTED →
2 Consecutive
Const. strides**

intruction pc%1024	last stride	prev address	detected
	<i>4 bytes</i>	<i>8 bytes</i>	<i>1 bit</i>

CONSTANT STRIDE DETECTING OPEN/CLOSE PAGE PREDICTOR



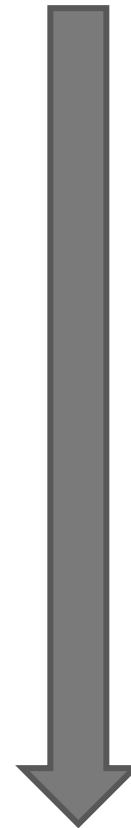
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**GLOBAL HISTORY- BASED
CLOSE PAGE PREDICTOR**



**COMMAND
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GLOBAL HISTORY- BASED CLOSE PAGE PREDICTOR

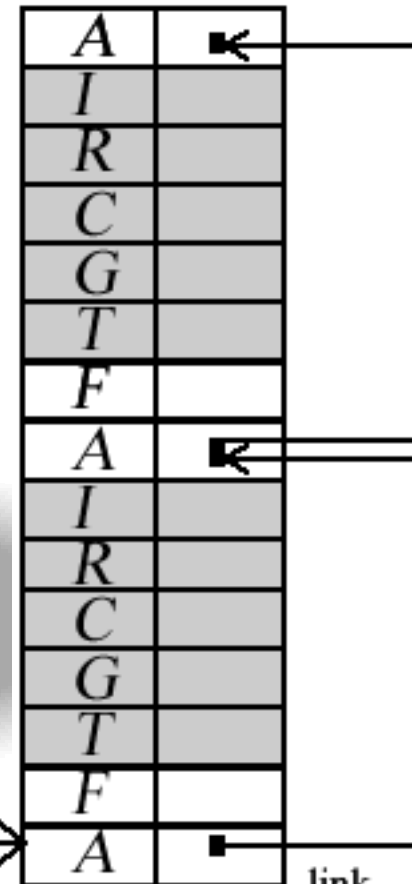
Thread id	Instruction PC XOR Address
2 bits	8 bits

Index Table

A	■
B	
C	
D	

Index Table: 1024 entries
 GHB: 512 entries

GHB



BREADTH

DEPTH

head ptr

FIFO

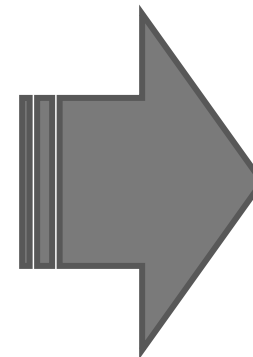
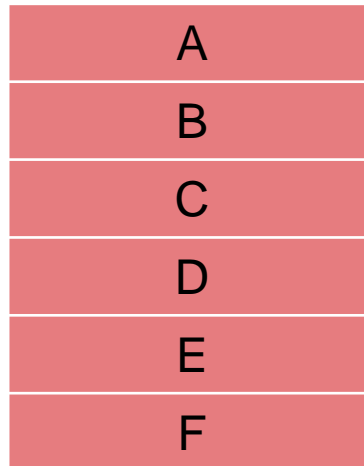
link

GLOBAL HISTORY- BASED CLOSE PAGE PREDICTOR

Optimal Configuration:

- Breadth : 3
- Depth : 20

Address,
a



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MEMORY REQUIREMENTS

MEMORY REQUIREMENTS FOR SCHEDULER

Entity	Size
Isused	$16*16*32*2B=16KB$
Stride Table	$1024*(12B+1b)=(12K+128)B$
ToBeIssued	$16*20B=320B$
GHB	$512*32B=16KB$
Index Table	$1024*8B=8KB$
Total	$(52K+448)B$

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EXPERIMENTAL RESULTS

– CONFIGS USED

Parameter	1channel.cfg	4channel.cfg
Processor clock speed	3.2 GHz	3.2 GHz
Processor ROB size	128	160
Processor retire width	2	4
Processor fetch width	4	4
Processor pipeline depth	10	10
Memory bus speed	800 MHz (plus DDR)	800 MHz (plus DDR)
DDR3 Memory channels	1	4
Ranks per channel	2	2
Banks per rank	8	8
Rows per bank	32768 × NUMCORES	32768 × NUMCORES
Columns (cache lines) per row	128	128
Cache line size	64 B	64 B
Address bits (function of above params)	32+log(NUMCORES)	34+log(NUMCORES)
Write queue capacity	64	96
Address mapping	row:rank:bank:chnl:col:blkoff	row:col:rank:bank:chnl:blkoff
Write queue bypass latency	10 cpu cycles	10 cpu cycles

WORKLOADS

No.	Workload
1	MTc
2	bl-bl-fr-fr
3	c1-c1
4	c1-c1-c2-c2
5	c2
6	fa-fa-fe-fe
7	fl-sw-c2-c2
8	st-st-st-st
9	fl-fl-sw-sw-c2-c2-fe-fe
10	fl-fl-sw-sw-c2-c2-fe-fe- bl-bl-fr-fr-c1-c1-st-st

BENCHMARK TRACES

Trace	Abbreviation
PARSECs blackscholes	bl
PARSECs facesim	fa
PARSECs ferret	fe
PARSECs fluidanimate	fl
PARSECs freqmine	fr
PARSECs stream	st
PARSECs swaptions	sw
Server-class transaction processing workload -1	c1
Server-class transaction processing workload -2	c2
PARSECs canneal (4 threads)	MTc

METRIC USED

Speculation Accuracy

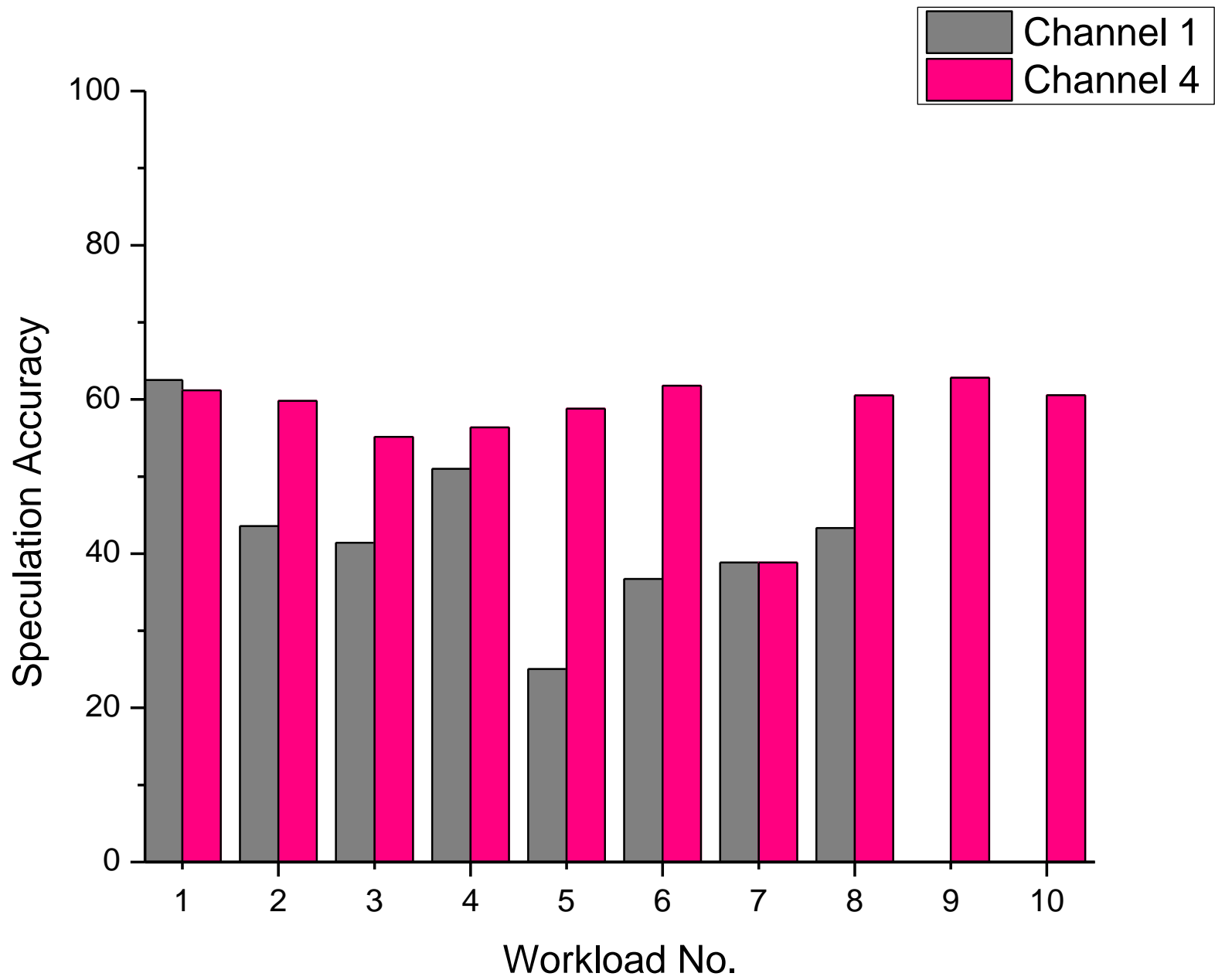
$$\textit{Speculation Accuracy} = \frac{\textit{Accurate Speculation}}{\textit{Total Speculation}} \times 100$$



Next Request to bank
Is a different row than
That closed



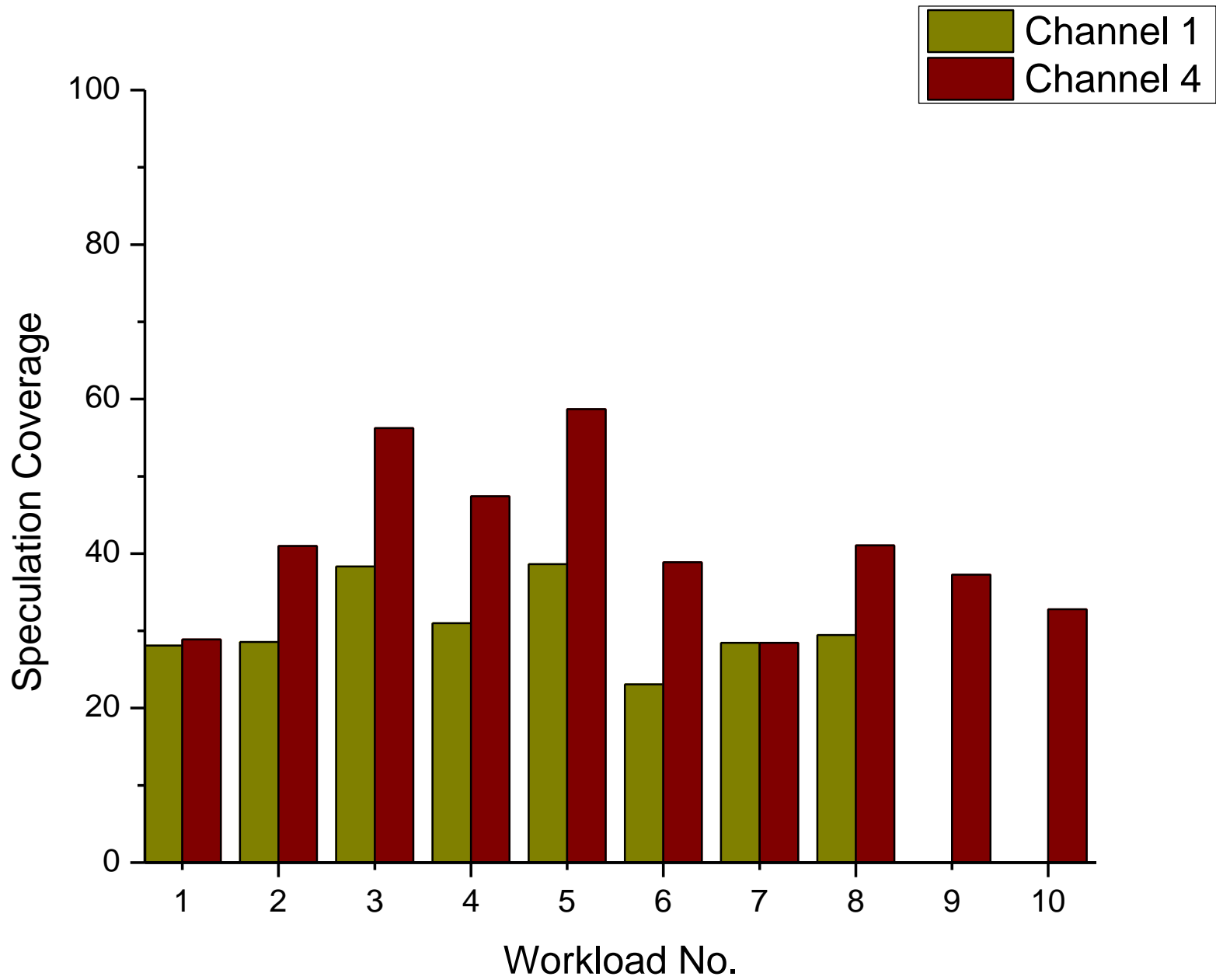
Next Request to bank
Is a ROW BUFFER HIT



METRIC USED

Speculation Coverage

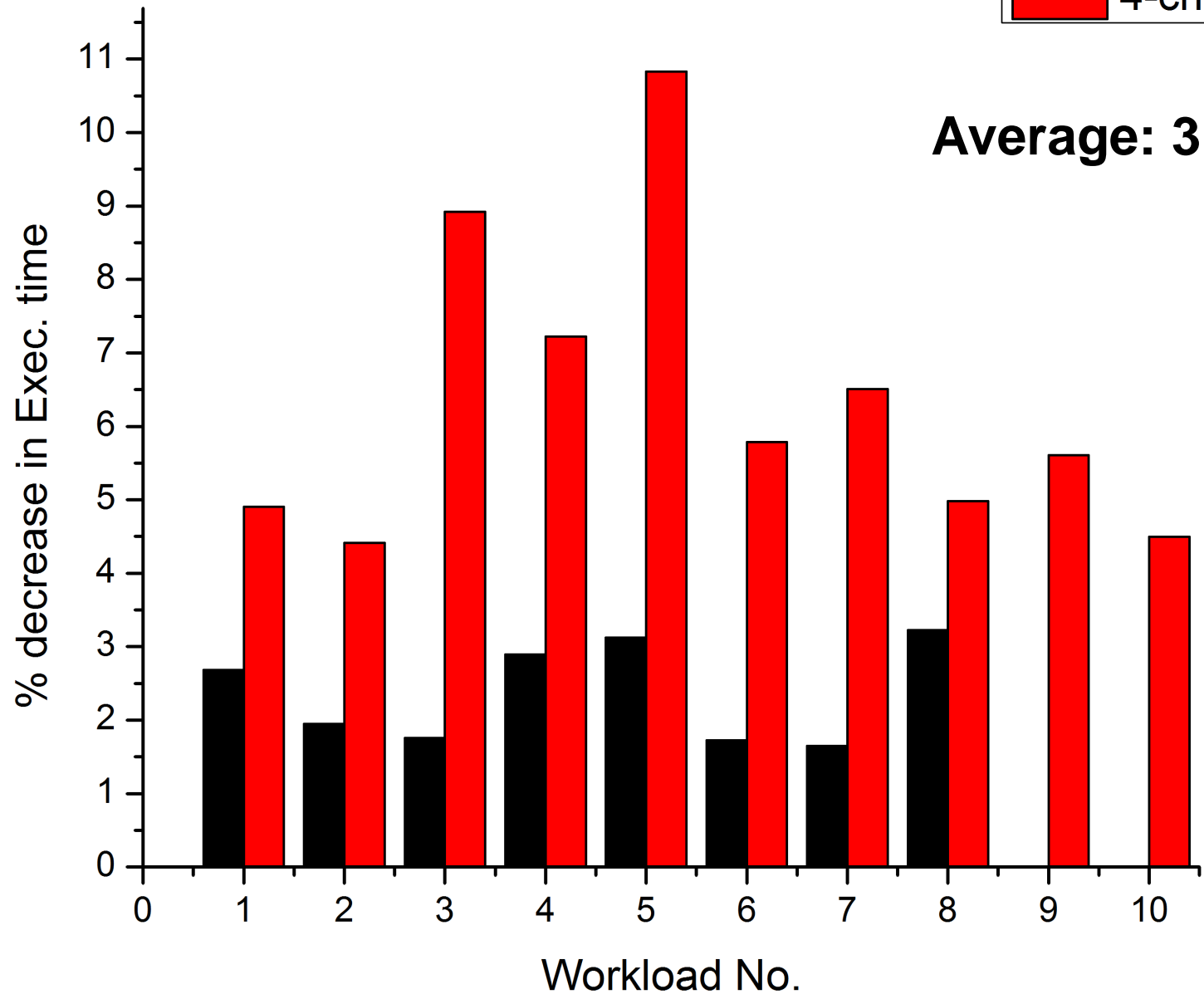
$$\textit{Speculation Coverage} = \frac{\textit{Accurate Speculation}}{\textit{Total ACTs and PREs}} \times 100$$



METRIC USED

% Decrease in Execution Time (compared to FR-FCFS)

$$\% \text{ Decrease in Exec. Time} = \frac{E_{FR-FCFS} - E}{E_{FR-FCFS}} \times 100$$



Average: 3.97%

THANKS

Prof. Mikko Lipasti

QUESTIONS