Lecture: Cache Hierarchies

• Topics: cache access basics, example problems on cache access
Accessing the Cache

Direct-mapped cache: each address maps to a unique address

Byte address

101000

Offset

8 words: 3 index bits

Data array

Sets

8-byte words
The Tag Array

Direct-mapped cache: each address maps to a unique address.
Increasing Line Size

A large cache line size $\rightarrow$ smaller tag array, fewer misses because of spatial locality

32-byte cache line size or block size
Set associativity $\rightarrow$ fewer conflicts; wasted power because multiple data and tags are read.

10100000

Tag array

Tag

Byte address

Compare

Way-1

Data array

Way-2
Problem 2

• Assume a direct-mapped cache with just 4 sets. Assume that block A maps to set 0, B to 1, C to 2, D to 3, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A
Problem 2

• Assume a direct-mapped cache with just 4 sets. Assume that block A maps to set 0, B to 1, C to 2, D to 3, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A
M MH MM H MM HM HMM M M M
Problem 3

• Assume a 2-way set-associative cache with just 2 sets. Assume that block A maps to set 0, B to 1, C to 0, D to 1, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A
Problem 3

• Assume a 2-way set-associative cache with just 2 sets. Assume that block A maps to set 0, B to 1, C to 0, D to 1, E to 0, and so on. For the following access pattern, estimate the hits and misses:

A B B E C C A D B F A E G C G A
M MH M MH MM HM HMM M H M
Problem 4

• 64 KB 16-way set-associative data cache array with 64 byte line sizes, assume a 40-bit address

• How many sets?

• How many index bits, offset bits, tag bits?

• How large is the tag array?

Equations:
Data array size (cache size) = \#sets \times \#ways \times \text{blocksize}
Tag array size = \#sets \times \#ways \times \text{tagsize}
Index bits = \log_2 (\#sets)
Offset bits = \log_2 (\text{blocksize})
Tag bits + index bits + offset bits = address width
Problem 4

- 64 KB 16-way set-associative data cache array with 64 byte line sizes, assume a 40-bit address

- How many sets? 64

- How many index bits (6), offset bits (6), tag bits (28)?

- How large is the tag array (28 Kb)?
Problem 5

• 8 KB fully-associative data cache array with 64 byte line sizes, assume a 40-bit address

• How many sets? How many ways?

• How many index bits, offset bits, tag bits?

• How large is the tag array?
Problem 5

- 8 KB fully-associative data cache array with 64 byte line sizes, assume a 40-bit address
- How many sets (1)? How many ways (128)?
- How many index bits (0), offset bits (6), tag bits (34)?
- How large is the tag array (544 bytes)?

Equations:
Data array size (cache size) = #sets x #ways x blocksize
Tag array size = #sets x #ways x tagsize
Index bits = log₂ (#sets)
Offset bits = log₂ (blocksize)
Tag bits + index bits + offset bits = address width