Chapter **5** Virtuoso Layout Editor

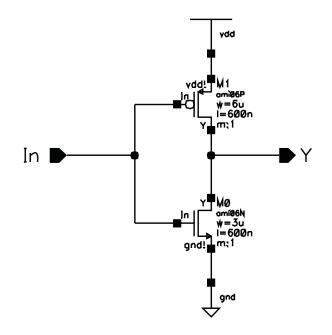


Figure 5.1: Inverter schematic

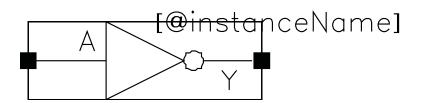


Figure 5.2: Inverter symbol

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/home/e	1b/IC_CAI)/cadence1.5/	cds.lib

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Figure 5.3: Dialog for creating a Layout View of the inverter cell

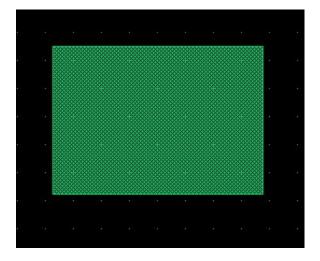


Figure 5.4: Initial nactive rectangle

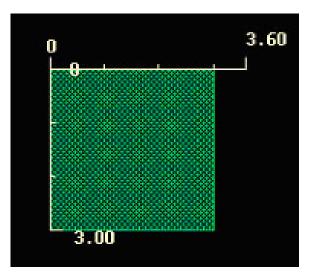


Figure 5.5: nactive rectangle with measurement rulers

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Delta X	1.5	Delta Y	1. §
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Figure 5.6: Create contact dialog box

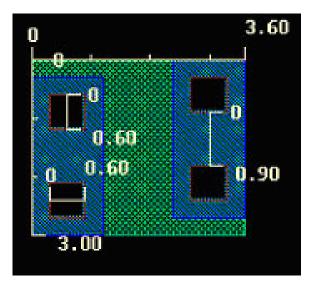


Figure 5.7: nactive showing source and drain connections

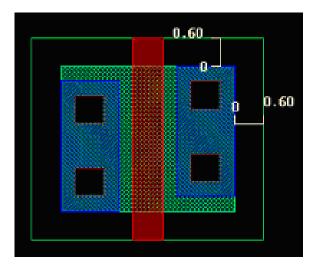


Figure 5.8: Nmos transistor 3μ wide and 0.6μ long

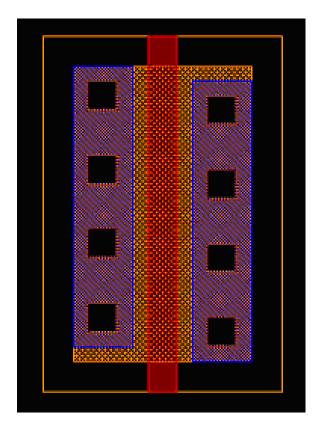


Figure 5.9: A pmos transistor 6μ wide and 0.6μ long

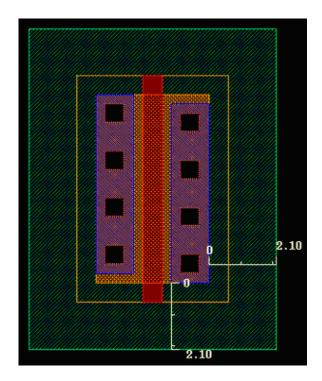


Figure 5.10: A pmos transistor inside of an NWELL region

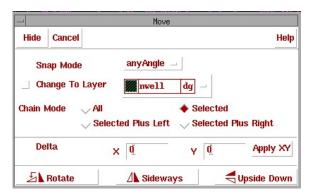


Figure 5.11: Extra features dialog box in move mode

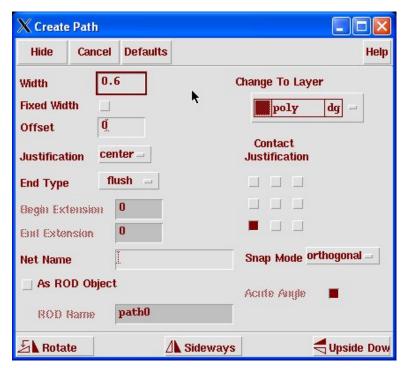


Figure 5.12: Dialog box for the path command

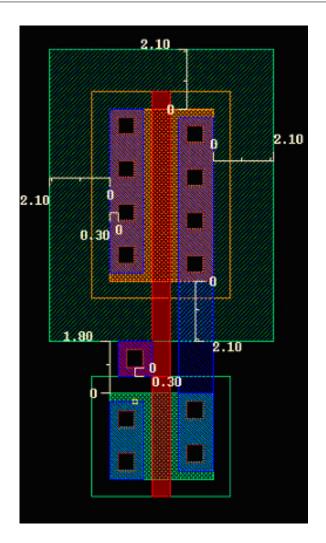


Figure 5.13: Inverter layout with input and output connections made

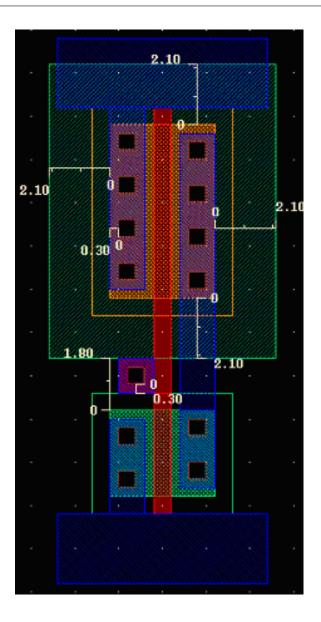


Figure 5.14: Inverter layout with power supply connections

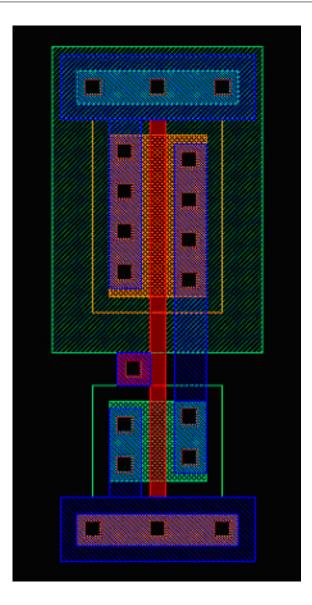
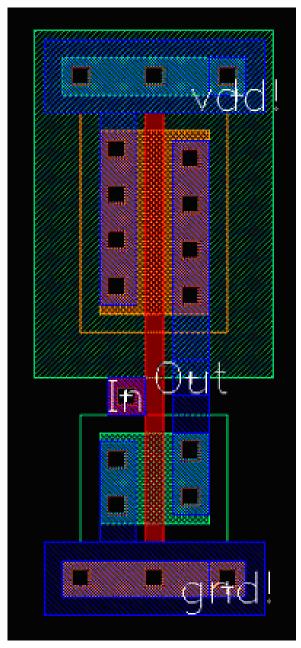


Figure 5.15: Inverter layout with well and substrate connections



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Figure 5.16: Shape pin dialog box



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Figure 5.17: Final inverter layout

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Figure 5.18: Layout with four inverter instances

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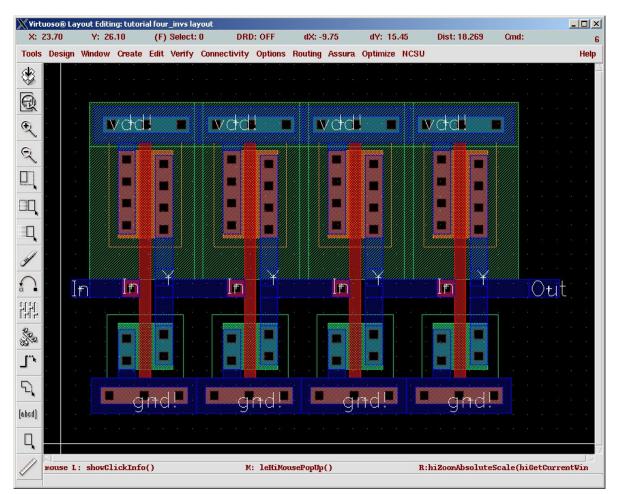


Figure 5.19: Layout with four inverter instances expanded to see all levels of layout

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Libr	ary Name	tutorial	Browse
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Figure 5.20: Submit Plot dialog box

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_ Queu _ Send	Of Copies e Plot Dat Plot Only Log To	ta At		Directory /uss	1

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Figure 5.21: Plot Options dialog box

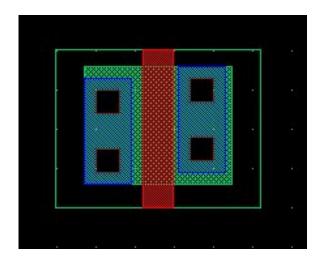


Figure 5.22: Nmos transistor layout (with DRC errors)

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XDRC	1	1	1		
ок	Cancel	Defaults	Apply		Help
Checkinį	j Method	🔶 flat	hierarc	ical 🔷 hier w/o optimiza	ation
Checkinį	ı Limit	🔶 full	◇ increment	ntal 🔷 by area	
		Coontin	nate		Sel by Cursor
Switch I	Names				Set Switches
Run-Spe	cific Comr	nand File			
Inclusior	i Limit		1000	Limit Rule Errors	0
Join Net	s With San	ne Name		Limit Run Errors	0
Echo Co	mmands				
Rules Fil	e		divaDRO	.rul	
Rules Lil	orary		U_Te	chLib_ami06	
					27

Figure 5.23: DIVA DRC control window

Xicfb - Log: /home/elb/CD5.log				
File Tools Options			Help	1
1 (SCMOS Rule 4.2)	gate enclosure of active: 0.60 w select overlap of active: 0.60 w active contact to transistor gat nd	m		
1 (SCMOS Rule 4.4) n select spacing: 0.60 w]			
mouse L: Enter Point	M: Pop-up Menu	R:		
Select the figure to be stretche	d:			

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Figure 5.24: Results from the DRC in the CIW window

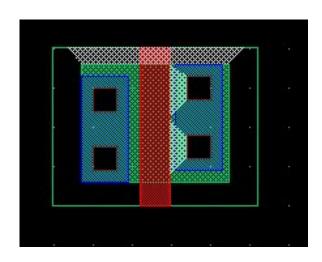
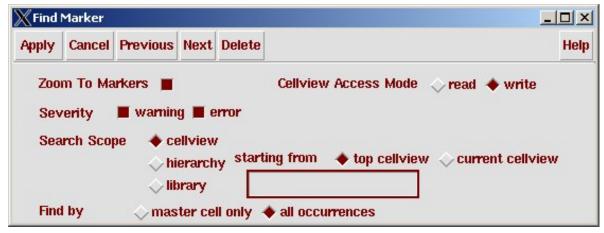


Figure 5.25: Nmos transistor layout (with DRC errors flagged)

_	
Help	6
	Help

Figure 5.26: Explanation of DRC violation



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Figure 5.27: Finding all DRC violations

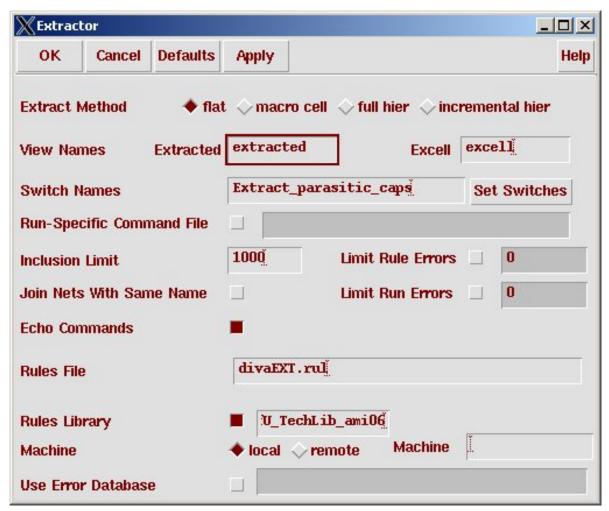


Figure 5.28: DIVA extraction control window

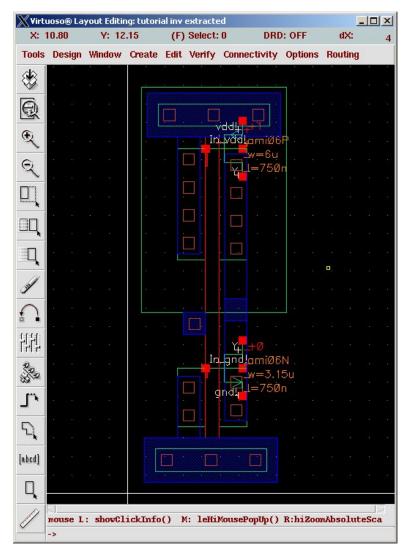


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Figure 5.29: DIVA extraction special switches

💥 icfb - Lo	g: /home/elb/CD5.log		X
File Too	s Options	Help	1
executing executing executing Extraction CPU ********* Total	: saveDerived(metal1 ("metal1" "net") cell_v: : saveDerived(metal2 ("metal2" "net") cell_v: : saveDerived(via ("via" "net") cell_view) : saveDerived(metal3 ("metal3" "net") cell_v: : saveDerived(via2 ("via2" "net") cell_v: n startedMon Aug 14 16:27:32 2006 completedMon Aug 14 16:27:33 2006 IME = 00:00:00 TOTAL TIME = 00:00:01 Summary of rule violations for cell "inv 1 errors found: 0 p tutorial/inv/extracted	.ew) ew)	21 IS
<u></u>			
I			
mouse L:	showClickInfo() M: leHiMousePop	<pre>Jp() R: setExtForm()</pre>	
->			

Figure 5.30: DIVA extraction result in the CIW



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Figure 5.31: Extracted view of the inverter

🕻 Artist L¥S					
Commands			Help 5		
Run Directory	LVS		Browse		
Create Netlist	schematic	extracted			
Library	tutorial	tutorial			
Cell	inv	inv			
View	schematič	extracted			
	Browse Sel by Cursor	Browse Sel	by Cursor		
Rules File	divaLVS.rul		Browse		
Rules Library	UofU_TechLib_ami06				
LVS Options	Rewiring	Device Fixin	g		
	Create Cross Reference	Terminals			
Correspondence	File lvs_corr_file		Create		
Switch Names	,		Ī		
Priority 0	Run local 🖃 🎽				
Run	Output Error Display	Monitor	Info		
	Parasitic Probe Build	Analog Bu	Sector of the		

Figure 5.32: DIVA LVS control window

🗙 Artist L¥S F	orm Contents Different	
OK Canc	el	Help
The selected	LVS Run directory does not match the Run Form.	
Use	Form Contents 😞 Run Directory Contents	
Differences:	Extracted Library Name: tutorial Extracted Cell Name: inv	
	Extracted View Name: extracted Schematic Library Name: tutorial	
	Schematic Cell Name: inv	-
	Schematic View Name: schematic	

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Figure 5.33: DIVA LVS Control Form

	ify LVS Rules			
ок	Cancel		Help	
Lânary:		tutorial		
Allow F	ET Series Permutation	•		
Combine Parallel FETs				
Combine Parallel Resistors				
Combin	ne Series Resistors			
Combin	ne Parallel Capacitors	•		
Combin	ne Series Capacitors			
Compare FET Parameters				
lgnore FET Body Terminal				
Compa	re Capacitor Parameters			
Compa	re Resistor Parameters			

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Figure 5.34: NCSU form to modify LVS rules



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Figure 5.35: DIVA LVS completion indication

X/home/elb/IC_CAD/cadencetest/LVS/si.out - 0 × File Help 6 @(#)\$CDS: LVS.exe version 5.1.0 07/23/2006 23:38 (cicln01) \$ Command line: /www.soc/facility/cad_tools/Cadence/IC51411SR200607280110/tools/dfII/bin/ Like matching is enabled. Net swapping is enabled. Using terminal names as correspondence points. Compiling Diva LVS rules... Net-list summary for /home/elb/IC_CAD/cadencetest/LVS/layout/netlist count 4 nets 4 terminals pmos 1 1 nmos Net-list summary for /home/elb/IC_CAD/cadencetest/LVS/schematic/netlist count 4 nets 4 terminals 1 pmos 1 nmos Terminal correspondence points N2 N2 In N3 NI gnd! NI NŪ vdd! Devices in the rules but not in the netlist: cap nfet pfet nmos4 pmos4 The net-lists failed to match. layout schematic instances un-matched 0 0 0 0 rewired 0 0 size errors 0 0 pruned active 2 2 total 2 2 nets un-matched 0 0 merged 0 0 pruned 0 0 active 4 4 total 4 4

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Figure 5.36: DIVA LVS output

```
X/home/elb/IC_CAD/cadencetest/LVS/si.out
                                                                                   - 0 ×
File
                                                                                Help
                                                                                       6
                                 0
                                         0
        pruned
        active
                                 4
                                         4
        total
                                 4
                                         4
                                 terminals
        un-matched
                                 1
                                         1
        matched but
        different type
                                         0
                                 0
        total
                                 4
                                         4
Probe files from /home/elb/IC_CAD/cadencetest/LVS/schematic
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
T -1 Out /Out
? Terminal Out in the schematic is not present in the layout.
prunenet.out:
prunedev.out:
audit.out:
Probe files from /home/elb/IC_CAD/cadencetest/LVS/layout
devbad.out:
netbad.out:
mergenet.out:
termbad.out:
T -1 Y /Y
? Terminal Y in the layout is not present in the schematic.
prumenet.out:
prunedev.out:
audit.out:
```

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Figure 5.37: DIVA LVS output (scrolled)

ок	Cancel	Defaults	Apply		Hel
Run Info	Log F	ile Outpu	ıt		
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	Audit	Merged I	Nets P	runed Nets	Pruned Devices
Extracted	Netlis	t Bad De	evices	Bad Nets	Bad Terminals
	Audit	Merged I	Nets P	runed Nets	Pruned Devices

Figure 5.38: DIVA LVS Run Information window