# 250P: Computer Systems Architecture

# Lecture 3: Basics of pipelining

Anton Burtsev January, 2019

# Building a Car

Time

# Building a Car



# The Assembly Line



Time

Break the job into smaller stages

### **Clocks and Latches**



### **Clocks and Latches**



#### Some Equations

- Unpipelined: time to execute one instruction = T + Tovh
- For an N-stage pipeline, time per stage = T/N + Tovh
- Total time per instruction = N (T/N + Tovh) = T + N Tovh
- Clock cycle time = T/N + Tovh
- Clock speed = 1 / (T/N + Tovh)
- Ideal speedup = (T + Tovh) / (T/N + Tovh)
- Cycles to complete one instruction = N
- Average CPI (cycles per instr) = 1



Source: H&P textbook <sup>8</sup>

#### Use the PC to access the I-cache and increment PC by 4



Read registers, compare registers, compute branch target; for now, assume branches take 2 cyc (there is enough work that branches can easily take more)



#### ALU computation, effective address computation for load/store



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#### Memory access to/from data cache, stores finish in 4 cycles



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#### Write result of ALU computation or load into register file



#### **RISC/CISC** Loads/Stores

#### Thank you!

#### AM vs. GM

- GM of IPCs = 1 / GM of CPIs
- AM of IPCs represents thruput for a workload where each program runs sequentially for 1 cycle each; but high-IPC programs contribute more to the AM
- GM of IPCs does not represent run-time for any real workload (what does it mean to multiply instructions?); but every program's IPC contributes equally to the final measure

- "Speedup" is a ratio = old exec time / new exec time
- "Improvement", "Increase", "Decrease" usually refer to percentage relative to the baseline
  = (new perf – old perf) / old perf
- A program ran in 100 seconds on my old laptop and in 70 seconds on my new laptop
  - What is the speedup?
  - What is the percentage increase in performance?
  - What is the reduction in execution time?