

The ‘Test Model-checking’ Approach to the Verification of Formal Memory Models of Multiprocessors *

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Abstract

We offer a solution to the problem of verifying formal memory models of processors by combining the strengths of model-checking and a formal testing procedure for parallel machines. We characterize the formal basis for abstracting the tests into test automata and associated memory rule safety properties whose violations pinpoint the ordering rule being violated. Our experimental results on Verilog models of a commercial split transaction bus demonstrates the ability of our method to effectively debug design models during early stages of their development.

Keywords: Formal memory models, shared memory multiprocessors, formal testing, model-checking.