Table of Contents

- Preface
- Inverter Gate Design
  - Inverter gate schematic and symbol
  - Inverter gate simulation
  - Inverter gate layout and results of verification
- NAND2 Gate Design
  - NAND2 gate schematic and symbol
  - NAND2 simulation
  - NAND2 gate layout and results of verification
- NAND3 Gate Design
  - NAND3 gate schematic and symbol
  - NAND3 simulation
  - NAND3 gate layout and results of verification
- D Flip-Flop Design
  - D Flip-Flop schematic and symbol
  - D Flip-Flop simulation
  - D Flip-Flop layout and results of verification
- D Flip-Flop P/C Design
  - D Flip-Flop P/C schematic and symbol
  - D Flip-Flop P/C simulation
  - D Flip-Flop P/C layout and results of verification
Preface

• This document provides the information on how to design D Flip-Flop schematic and layout.

• D Flip-Flop is designed based on MOSIS SCMOS layout rules.

• If you want to get more information, please refer to the related documents as below.
  – MyCAD Tutorial:
    Learn how to use schematic and layout editor.
  – MySpice Tutorial:
    Learn about simulating a circuit.
  – MyChip Pro Verification Reference Manual:
    Look up specific verification commands.
Inverter schematic and symbol

**Schematic**

- **PMOS**
  - L = 0.2um
  - W = 1.6um

- **NMOS**
  - L = 0.2um
  - W = 0.6um

**Logic Symbol**

**Truth Table**

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
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<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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Inverter Simulation

IN

OUT
Inverter layout and results of verification

Layout

DRC result

LVS result
NAND2 schematic and symbol

Logic Symbol

<table>
<thead>
<tr>
<th>IN0</th>
<th>IN1</th>
<th>OUT</th>
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<tbody>
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<td>1</td>
</tr>
<tr>
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<tr>
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</tbody>
</table>

Schematic
NAND2 Simulation

IN0

IN1

OUT
NAND2 layout and results of verification

Layout

DRC result

LVS result
### NAND3 Schematic and Symbol

#### Logic Symbol

![NAND3 Logic Symbol]

#### Truth Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
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<tbody>
<tr>
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</tbody>
</table>

#### Schematic

![NAND3 Schematic Diagram]
NAND3 layout and results of verification

Layout

DRC result

LVS result
D Flip-Flop schematic and symbol

Logic Symbol

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
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<tbody>
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<td>CLK</td>
<td>D</td>
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<td>0</td>
</tr>
<tr>
<td>↑ 1</td>
<td>1</td>
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</tbody>
</table>

Truth Table

Schematic
D Flip-Flop Simulation

Clock

D (input)

Q (output)
D Flip-Flop layout and results of verification

Layout

DRC result

LVS result
D Flip-Flop with Preset and Clear schematic and symbol

**Logic Symbol**

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
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<tbody>
<tr>
<td>CLK</td>
<td>CLR</td>
</tr>
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</tr>
<tr>
<td>↑</td>
<td>1</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
</tr>
</tbody>
</table>

**Schematic**
D Flip-Flop with Preset and Clear Simulation (1/2)

Clock

D (input)

Preset

Clear
D Flip-Flop with Preset and Clear Simulation (2/2)

Q (output)

Q_bar (output)
D Flip-Flop with Preset and Clear
layout and results of verification

Layout

DRC result

LVS result
The End