

8 Bit Digital-to-Analog Converter

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8 Bit DAC

Project Description:

For this project, an 8 bit digital-to-analog converter was designed. It was designed following the R-2R ladder method (As seen on page 472 in Johns & Martin). The circuit is run off of 3 volt and -3 volt power supplies. The circuit will take in 8 digital inputs ($0 = -3$ volts, $1 = 3$ volts) and use them to output an analog signal between 0 and 3 volts. The digital inputs will be named $b1 - b8$, and the output will be named V_o . The expected maximum frequency is 10 MHz. It is expected that the step size will be nearly linear. The expected power dissipation is 10 mW. The op-amp was designed by our team and has traits that are essential to a digital-to-analog converter (DAC).

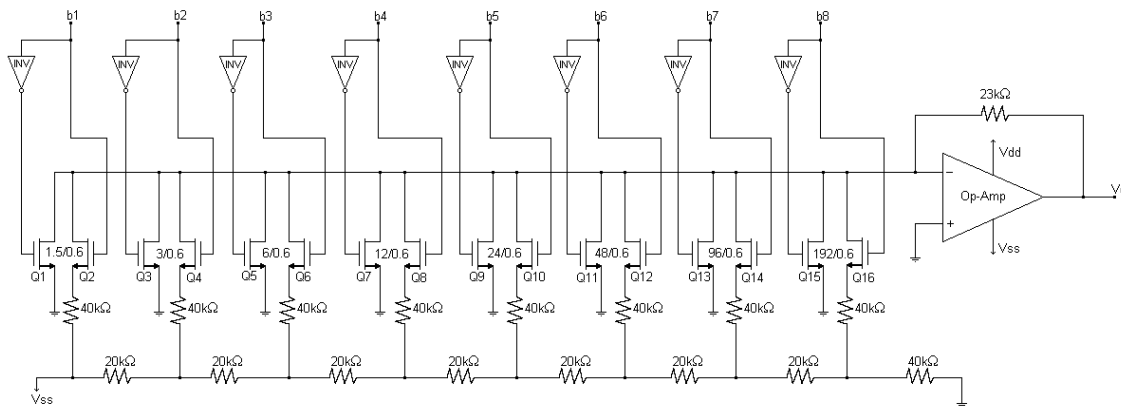


Figure 1 DAC schematic

The op-amp is derived from a simple two-stage op amp. A cascaded current mirror is used to generate the bias current that is necessary. In order to provide a good rail to rail voltage, a pmos source-follower circuit is used for the output stage on the op-amp. This is essential in our design, because we want a high rail that is as close to 3 volts as possible. The op-amp utilizes a compensation capacitor and a transistor to ensure a proper phase margin.

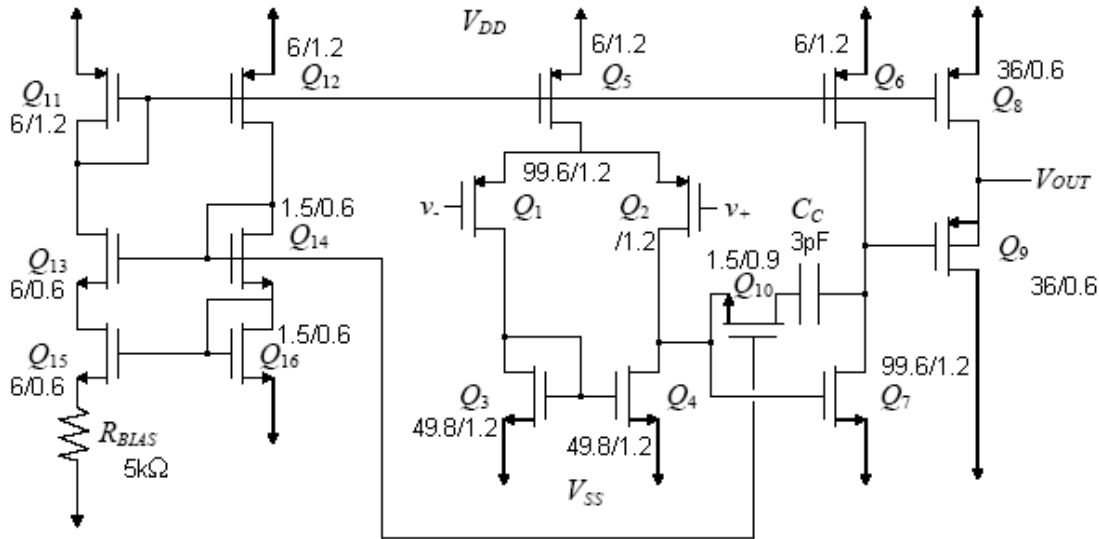


Figure 2 Op-Amp schematic

To implement the switches that the digital inputs control in the circuit, 2 nmos mosfets and 1 inverter per switch are used. Each set of transistors is sized in a way that will help the proper amount of current to flow when needed. The least significant bit (lsb) has a width of 1.5 μm , while the most significant bit (msb) has a width of 192 μm . Since the voltage step of each bit is twice the amount of the preceding bit, the transistors are sized in the same manner. The lsb has transistors sized 1.5 μm , bit 2 has transistors sized 3 μm , and so forth. This is done so that all step sizes will be approximately the same.

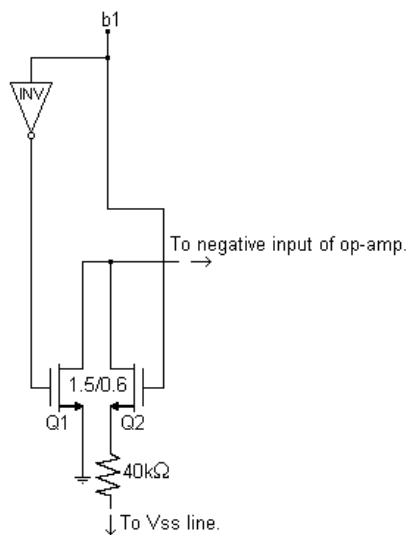


Figure 3 Switch for bit 1

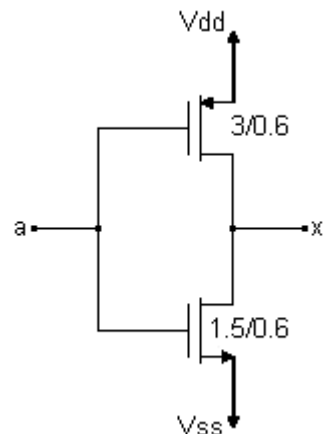


Figure 4 Inverter

Simulated Circuit Description:

To simulate the circuit, a load is added to the output. This load has a capacitance of 20 pF and resistance of 10 M Ω in parallel. 3 volts is used for V_{dd} and -3 volts is used for V_{ss}. Using this, we found that the lsb generates a step size of approximately 40 mV.

To check for the maximum frequency, b1 – b8 are pulsed from -3 volts to 3 volts, and then back to -3 volts. The settling time is found by measuring how long it takes the DAC to transition from 0 volts to 2.8 volts when the input changes from “00000000” to “11111111”. Since the output voltage only has to be within half of the lsb’s step size from the positive rail voltage, 2.8 volts is used. This test can be seen in figure 1. Once the settling time is found, the maximum frequency can be easily calculated. By computing 1 / (settling time) the maximum frequency is found at 12 MHz. This is above our specification.

Next the power consumption is tested. This is done by running the circuit, and displaying the current flowing through each of the power supplies. This test is performed while the digital inputs are all pulsing from 0 to 1. When the inputs are ‘0’, the power dissipation is approx. 9 mW. When the inputs are ‘1’, the power dissipation is approx 1.8 mW. These values are below our expected values.

To obtain a reasonable output range, the resistor values had to be tweaked from the original design. Many simulations were conducted with different values of R, 2R, and R_f. The values that gave us the best results are as follows:

$$\begin{aligned}R &= 20\text{K } \Omega \\2R &= 40\text{K } \Omega \\R_f &= 23\text{K } \Omega\end{aligned}$$

Testing Strategies:

This chip has not been intended to be fabricated. If it were to be fabricated, the way the chip would be tested would be fairly simple.

To test the circuit for functionality, a simple test counting from 0 to 255. This should show an increment for each step. The expected output would be a wave from 0 volts to 3 volts with 256 steps. If this DAC were an ideal one, each step size would be identical.

To test for maximum frequency the test would be done the same as we did in our simulations.

Power Dissipation could be measured by measuring the currents each of the power supplies provides.

Limitations, Trade-Offs, and Future Improvements:

Equal step size is one factor that limits this DAC. To obtain an equal step size, the transistor sizes would need to be tweaked. This will be time consuming and we did not have the time to do it. The way we sized the transistors is a good approximate, but to be exact, more time would be needed.

This DAC does not reach 0 volts or 3 volts exactly. Due to time constraints, we could not make the op-amp as ideal as possible. This is kind of an important thing to fix in a DAC. If this chip was intended for fabrication, more time would need to be spent making the output range more ideal.

One trade-off that was encountered was the ability of the step sizes to be equal and have the output range where it was desired. When trying to make the step sizes more equal, we noticed that the low output became higher. To keep the low output as close to 0 volts as possible, the resistor values had to be kept at the values we listed above.

Due to time constraints, the layout of the chip is not as compact as it could be. One future improvement would be to make the layout more compact. Chip size is worth lots of money, so this would be a great improvement that would make the chip fabrication cheaper.

Another improvement that would greatly benefit this chip would be to provide each switch with an equal bias current. This would improve step-size and make it possible to make the switch transistors to be smaller. This would be a great improvement to the R-2R ladder DAC.