

Robert Allan Thacker

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OBJECTIVE: Research position in the design of VLSI systems.

EDUCATION:

University of Utah, Salt Lake City, Utah (1996-present)
M.S. degree in Computer Science (expected spring 1998)
Thesis: Implicit Methods for Timed Circuit Synthesis
B.S. degree in Computer Engineering (June 1996)
B.S. degree in Computer Science (June 1996)
B.A. degree in Spanish (June 1996)

EMPLOYMENT EXPERIENCE:

Research Assistant, Professor Chris J. Myers, *University of Utah* (1996-present)

- Developed algorithms using implicit methods for timed circuit synthesis.
- Applied implicit methods to the problem of exploring large state spaces.

System Administrator, Asynchronous Design Group, *University of Utah* (1996-present)

- Configure and maintain a heterogeneous network of Unix-based workstations.

Research Assistant, Professor Ganesh C. Gopalakrishnan, *University of Utah*
(1995-1996)

- Developed methods for transforming Verilog code into Petri-net based specifications.
- Implemented a Verilog to Petri-net compiler.

AWARDS:

Fourth place, student VLSI design contest, *U. of Utah/U. of Michigan* (1997)

Phi Beta Kappa National Honor Society (1996)

Tau Beta Pi National Honor Society (1996)

PRESENTATIONS:

R. Thacker and C. Myers. Synthesis of timed circuits using BDDs, at the
International Workshop on Logic Synthesis, 1997

OTHER TECHNICAL SKILLS:

Programming languages: C, C++, Pascal, Verilog, and VHDL

CAD tools: Cadence, Synopsis and Viewlogic