

Manjunath Shevgoor

CONTACT INFORMATION

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[Google Scholar Link](#)

RESEARCH INTERESTS

Computer Architecture: CPU Core Architecture, Memory Hierarchies, DRAM organization, Non-Volatile Memories, Data Prefetching.

EDUCATION

Ph.D. in Computer Engineering **August 2012 - October 2015**
University of Utah, Salt Lake City, USA
Advisor: Prof. Rajeev Balasubramonian

M.S. in Computer Engineering **August 2010 - July 2012**
University of Utah, Salt Lake City, USA
Advisor: Prof. Rajeev Balasubramonian

B.E. in Electronics and Communication **June 2002 - May 2006**
Visvesvaraya Technological University, Bangalore, India

PROFESSIONAL EXPERIENCE

Intel, Santa Clara, CA, USA *Silicon Architecture Engineer* **Nov 2015 - Current**
Worked on Intel's next generation architecture for the Big Core. Proposed and modelled architectural optimizations and predictors in the Load-Store unit.

Intel, Hillsboro, OR, USA *Intern* **Spring 2014**
Developed data prefetchers for applications exhibiting non-uniform delta patterns. Also built a DRAM simulator that runs inside the *Simics* full system simulator.

Advanced Micro Devices, Austin, TX, USA *Co-op Intern* **Summer 2011**
Worked on the Implementation and Physical Design of a power gated block of the Unified North Bridge of a client product using 32nm technology.

Advanced Micro Devices, Bangalore, India *Design Engineer II* **2008-2010**
Worked on Physical Design, including Synthesis, Place & Route, Timing Closure, Electrical Closure.

Montalvo Computer Systems, Bangalore, India *Design Engineer I* **2007-2008**
Automated Full Chip Timing Flows and built tools to do timing budgeting.

Softjin Technologies Pvt. Ltd., Bangalore, India *Design Engineer I* **2006-2007**
Developed an automated Design For Test methodology for Die Stacked 3D chips.

SELECTED PUBLICATIONS

ISPASS 2016- Best Paper Award *Addressing Service Interruptions in Memory with Thread-to-Rank Assignment*,
Manjunath Shevgoor, Niladrish Chatterjee, Rajeev Balasubramonian, Jung-Sik Kim
IEEE International Symposium on Performance Analysis of Systems and Software, Sweden, April 2016.

MICRO 2015 *Efficiently Prefetching Complex Address Patterns*,
Manjunath Shevgoor, Sahil Koladiya, Chris Wilkerson, Zeshan Chishti, Seth Pugsley, Rajeev Balasubramonian
48th Annual IEEE/ACM International Symposium on Microarchitecture, Hawaii, December 2015.

MICRO 2015 *Avoiding Information Leakage in the Memory Controller with Fixed Service Policies*,
Ali Shafiee, Akhila Gundu, Manjunath Shevgoor, Gita Sreekumar, Hardik Jain, Rajeev Balasubramonian, Mohit Tiwari
48th Annual IEEE/ACM International Symposium on Microarchitecture, Hawaii, December 2015.

ICCD 2015 *Improving Memristor Memory with Sneak Current Sharing*,
Manjunath Shevgoor, Naveen Muralimanohar, Rajeev Balasubramonian
33rd IEEE International Conference on Computer Design , New York City, October 2015.

MICRO 2013 *Quantifying the Relationship between the Power Delivery Network and Architectural Policies in a 3D-Stacked Memory Device*,
Manjunath Shevgoor, Jung-Sik Kim, Niladrish Chatterjee, Rajeev Balasubramonian, Al Davis, Aniruddha N.Udipi
46th International Symposium on Microarchitecture (MICRO-46), Davis, December 2013.

MICRO 2012 *Leveraging Heterogeneity in DRAM Main Memories to Accelerate Critical Word Access*,
Niladrish Chatterjee, Manjunath Shevgoor, Rajeev Balasubramonian, Al Davis, Zhen Fang, Ramesh Illikkal, Ravi Iyer
45th International Symposium on Microarchitecture (MICRO-45), Vancouver, December 2012.

HPCA 2012 *Efficient Scrub Mechanisms for Error-Prone Emerging Memories*,
Manu Awasthi, Manjunath Shevgoor, Kshitij Sudan, Rajeev Balasubramonian, Bipin Rajendran, Viji Srinivasan
18th International Symposium on High-Performance Computer Architecture (HPCA-18), New Orleans, February 2012.

HONORS AND
AWARDS

Graduate Research Fellowship, 2014. University of Utah.
Outstanding Achievement Award, 2007. Montalvo Computer Systems India Pvt. Ltd, India.
Performer of the Quarter, 2007. Softjin Technologies Pvt., Ltd., India.

SKILLS

Languages : C, C++, Perl, Python, Shell Scripting.