SUMANTH GUDAPARTHI

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Research Interests

Computer Architecture: Memory Hierarchies, Neural Network Accelerators, Near-memory Computing, Memory Security, ASIC, Machine Learning.

Education

Doctor of Philosophy (PhD), Computer Science
University of Utah
Utah, United States, Summer 2022 (expected)

Master of Technology (M.Tech), VLSI & Computer Engineering
International Institute of Information Technology (IIIT-H)
Hyderabad, India, 2015

Bachelor of Technology (B.Tech), Electrical & Electronics Engineering
GITAM University
Visakhapatnam, India, 2013

Professional Experience

Research Intern
Google
May 2020 – August 2020 Sunnyvale, CA, U.S.A
- Memory optimization, cache hierarchy analysis, and profiling of fleet data in Google datacenters.

Co-Op Engineer
Advanced Micro Devices (AMD) Research
May 2019 – August 2019 Santa Clara, CA, U.S.A
- Exploring Memory Security, and Process In Memory (PIM) architectures.

Research Assistant
(Advisor: Prof. Rajeev Balasubramonian)
University of Utah
August 2017 – Present Salt Lake City, Utah, U.S.A
- Currently exploring ASIC accelerator architectures for training and inference of Neural Networks.

Design Engineer R&D
Advanced Micro Devices (AMD)
May 2016 – June 2017 Hyderabad, India
- Client SoC system security verification and debugging.

Design Engineer R&D
Smarttrak Solar Systems
June 2015 – April 2016 Hyderabad, India
- Design a sun position tracker using Xilinx FPGAs.
- Designed an energy efficient VFD (variable frequency divider), and boost converter for a 0.5HP sun tracking module.

Industrial Trainee
Bharat Heavy Electronics Limited (BHEL)
May 2012 – June 2012 Hyderabad, India
- Study of Design aspects of a Turbo Generator.

Publications

1. **Sumanth Gudaparthi**, Lin Jia, Rajeev Balasubramonian, Srinivasan Parthasarathy, "A Versatile Accelerator for Computational Pathology Applications", International Symposium on Computer Architecture **(ISCA '22) (under-review).**
2. **Sumanth Gudaparthi**, Sarabjeet Singh, Surya Narayanan, Rajeev Balasubramonian, Visvesh Sathe, "CANDLES: Channel-Aware Novel Dataflow-Microarchitecture Co-Design for Low Energy Sparse Neural Network Acceleration", **to-appear** in the 28th IEEE International Symposium on High Performance Computer Architecture **HPCA-28**.
3. Edouard Giacomin, **Sumanth Gudaparthi**, Juergen Boemmels, Rajeev Balasubramonian, Francky Catthoor, Pierre-Emmanuel Gaillardon, "A Multiply-And-Accumulate Array for Machine Learning Applications Based on a 3D Nanofabric Flow", **to-appear** IEEE Transactions on Nanotechnology **TNANO-2021**
4. **Sumanth Gudaparthi**, Surya Narayanan and Rajeev Balasubramonian, "Wire-Aware Architecture and Dataflow for CNN Accelerators", In Proceedings of the 52st Annual IEEE/ACM International Symposium on Microarchitecture **(MICRO-52)**.
5. **Sumanth Gudaparthi**, Surya Narayanan and Rajeev Balasubramonian, "Moving CNN Accelerator Computations Closer to Data," 2018 1st Workshop on Energy Efficient Machine Learning and Cognitive Computing for Embedded Applications colocated with ASPLOS (**EMC2/ASPLOS-23**).
6. **Sumanth Gudaparthi**, and Rahul Shrestha, "Energy-Efficient VLSI Architecture Implementation of Bi-Modal Multi-Banked Register-File Organization", **VDAT-2017**.

Programming

Python | C | C++ | SQL | MPI | OpenMP | HTML/CSS | MIPS Assembly | Shell Scripting

HDLs

Verilog | System-Verilog

Tools & Simulators

CACTI | GPGPU-SIM | QuestaSim | Cadence (RC, Virtuoso, Encounter) | Xilinx ISE | Xilinx EDK | SPICE | Matlab | MCPAT Simulator

Academic Projects

- **SISCA: An SRAM In-Situ Computing hardware Accelerator for cognitive and machine learning applications.**
  - ⋆ Addresses the memory wall bottleneck of neural networks.
  - ⋆ Modified the SRAM architecture to accomodate in-situ multiplication operations.
  - ⋆ Designed a hierarchical memory architecture with SRAM and eDRAM for higher on-chip storage density.

  We tested the performance and energy efficiency of our architecture over AlexNet and VGG workloads against DaDianNao architecture.
- **Parallelizing CNNs Using MPI and OpenMP.**
  - ⋆ Exploit two different kinds of parallelism in CNNs: model parallelism and data parallelism.
  - ⋆ Implement model parallelism (parallel computation of neurons) using OpenMP, and data parallelism (parallel mini-batches of images) using MPI.
  - ⋆ Speedup of 2.3x is achieved over sequential execution.
- **Detection of fake user accounts in Twitter**
  - ⋆ Competitive project on Kaggle.
  - ⋆ Design space exploration of 7 different machine learning algorithms to find the optimal solution.
  - ⋆ Algorithms explored: various types of perceptron algorithms, Decision Trees, SVMs, Logistic Regressions, Naive Bayes, Bagged forest, Modified SVM over Trees (2 layer neural network).
- **Hardware Mechanism to capture reuse of register operands**⋆

  - ⋆ Register file caching is implemented to capture the reuse and locality of register operands.
  - ⋆ Implemented the conventional cache reuse and replacement policies for the register file cache.
- **A 5-stage pipelined 32 bit MIPS processor architecture.**⋆
  Developed the RTL for a conventional 5-state pipelined MIPS processor. The architecture handles structural hazards, as well as data hazards.
- **A 4-way set associative cache and direct mapped cache implementation in RTL.**
  Developed RTL for set associative and direct mapped caches with Least Recently Used (LRU) replacement policy.
- **NAND Flash Controller in RTL.**
- **A GPS and ZigBee based tracking system on Xilinx FPGAs.**
- **Design of a 16-Digit parallel decimal Multiplier in Cadence Virtuoso 180 nm.**
- **Implementation of APB and I2C bus protocols in RTL.**

⋆ *Code & Testbench*: Verilog, System-verilog
Synthesis: Cadence RC
Layout: Cadence Encounter

Awards & Scholarships

School of Computing Fellowship
University of Utah
August 2017 – May 2018

PG Scholarship GATE/GPAT
AICTE
August 2013 – April 2015

Merit-cum-Means Scholarship
GITAM University
July 2009 – May 2013

Graduate Aptitude Test Exam
GATE'13
February 2013
- Secured 52 rank in EE among 152,381 candidates.

Graduate Course Work

- Computer Architecture
- Neuromorphic Architecture
- Machine Learning
- Parallel Computing HPC
- Operating Systems
- Advanced VLSI design
- Embedded Systems

Teaching Mentor:

Foundations of Computer Science CS-1030, Fall 2021.
Computer Organization CS-3810, Spring 2020.
Computer Organization CS-3810, Spring 2019.

Organizational Experience

GradSAC: Graduate Student Advisory Committee
University of Utah
August 2018 – January 2020

- Involved in RPT (Retention, Promotion, and Tenure) process for faculties.
- Assisted graduate students during their tenure in grad school.
- Organized a number of social events and assisted in new graduate recruiting.

GUSAC: GITAM University Science Activity Center

GITAM University

July 2011 – November 2012

- Part of the team that developed GUSAC Power Generator: A miniature power plant that has been designed and established in North-eastern part of Andra Pradesh, India.
- Conducted workshops on embedded systems.
- Organized GUSAC Carnival'12, a technical fest of GITAM University.