Lecture: Large Caches, Virtual Memory

• Topics: large caches, NUCA, virtual memory intro, TLB/cache access

Upcoming Schedule:

HW 6 due: Oct 28 (Wed)
HW 7 due: Nov 11 (Wed)
HW 8 due: Nov 18 (Wed)
HW 9 due: Nov 30 (Mon)

Dec 2\textsuperscript{nd} – last day of class (review session)
Dec 7\textsuperscript{th} – final exam
Midterm Exam

• Questions 1, 3, 4, 7, 8
• Question 2: AM of IPC or HM of IPC?
• Question 9: full-fledged SWP
• Question 5A: nature of dependences/br/mem
• Question 5B: training, inference
• Question 6A: bypassing helps, fewer ld/st, save energy
• Question 6B: larger window size, issue width, latency, steering

• Average: 84.
• 92+ : Top 16
• 88+ : Top 32
• 79+ : Top 52
• 59+ : Top 62
Shared Vs. Private Caches in Multi-Core

- What are the pros/cons to a shared L2 cache?
Shared Vs. Private Caches in Multi-Core

• Advantages of a shared cache:
  ▪ Space is dynamically allocated among cores
  ▪ No waste of space because of replication
  ▪ Potentially faster cache coherence (and easier to locate data on a miss)

• Advantages of a private cache:
  ▪ small L2 $\rightarrow$ faster access time
  ▪ private bus to L2 $\rightarrow$ less contention
UCA and NUCA

- The small-sized caches so far have all been uniform cache access: the latency for any access is a constant, no matter where data is found.

- For a large multi-megabyte cache, it is expensive to limit access time by the worst case delay: hence, non-uniform cache architecture.
Large NUCA

Issues to be addressed for Non-Uniform Cache Access:

- Mapping
- Migration
- Search
- Replication
Shared NUCA Cache

A single tile composed of a core, L1 caches, and a bank (slice) of the shared L2 cache.

The cache controller forwards address requests to the appropriate L2 bank and handles coherence operations.

Memory Controller for off-chip access
Problem 1

- Assume a large shared LLC that is tiled and distributed on the chip. Assume 16 tiles. Assume an OS page size of 8KB. The entire LLC has a size of 32 MB, uses 64-byte blocks, and is 8-way set-associative. Which of the 40 physical address bits are used to specify the tile number? Provide an example page number that is assigned to tile 0.
Problem 1

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The cache has 64K sets, i.e., 6 block offset bits, 16 index bits, and 18 tag bits. The address also has a 13-bit page offset, and 27 page number bits. Nine bits (bits 14-22) are used for the page number and the index bits. Any four of those bits can be used to designate the tile number, say, bits 19-22. An example page number assigned to tile 0 is xxx…xxx0000xxx…xxx

bit 22  19
Virtual Memory

• Processes deal with virtual memory – they have the illusion that a very large address space is available to them

• There is only a limited amount of physical memory that is shared by all processes – a process places part of its virtual memory in this physical memory and the rest is stored on disk

• Thanks to locality, disk access is likely to be uncommon

• The hardware ensures that one process cannot access the memory of a different process
Address Translation

- The virtual and physical memory are broken up into pages.

8KB page size

Virtual address

- virtual page number
- page offset

Translated to physical page number

Physical address

- physical page number
- page offset

Physical memory
Memory Hierarchy Properties

• A virtual memory page can be placed anywhere in physical memory (fully-associative)

• Replacement is usually LRU (since the miss penalty is huge, we can invest some effort to minimize misses)

• A page table (indexed by virtual page number) is used for translating virtual to physical page number

• The memory-disk hierarchy can be either inclusive or exclusive and the write policy is writeback
Since the number of pages is very high, the page table capacity is too large to fit on chip.

A translation lookaside buffer (TLB) caches the virtual to physical page number translation for recent accesses.

A TLB miss requires us to access the page table, which may not even be found in the cache – two expensive memory look-ups to access one word of data!

A large page size can increase the coverage of the TLB and reduce the capacity of the page table, but also increases memory waste.
Problem 2

• Build an example toy virtual memory system. Each program has 8 virtual pages. Two programs are running together. The physical memory can store 8 total pages. Show example contents of the physical memory, disk, page table, TLB. Assume that virtual pages take names a-z and physical pages take names A-Z.
Problem 2

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Diagram:
- Processor
- TLB: a→A, c→C, m→M, z→Z
- Memory: A B C D M N O Z
- Page table:
  - a→A
  - b→B
  - c→C
  - d→D
  - e→E'
  - f→F'
  - g→G'
  - h→H'
- Disk: E'F' G'H' P'Q'
- Other Files
TLB and Cache

• Is the cache indexed with virtual or physical address?
  ➢ To index with a physical address, we will have to first look up the TLB, then the cache ➔ longer access time
  ➢ Multiple virtual addresses can map to the same physical address – can we ensure that these different virtual addresses will map to the same location in cache? Else, there will be two different copies of the same physical memory word

• Does the tag array store virtual or physical addresses?
  ➢ Since multiple virtual addresses can map to the same physical address, a virtual tag comparison can flag a miss even if the correct physical memory word is present
TLB and Cache
Virtually Indexed Caches

- 24-bit virtual address, 4KB page size → 12 bits offset and 12 bits virtual page number
- To handle the example below, the cache must be designed to use only 12 index bits – for example, make the 64KB cache 16-way
- Page coloring can ensure that some bits of virtual and physical address match
Cache and TLB Pipeline

Virtually Indexed; Physically Tagged Cache
Problem 3

• Assume that page size is 16KB and cache block size is 32 B. If I want to implement a virtually indexed physically tagged L1 cache, what is the largest direct-mapped L1 that I can implement? What is the largest 2-way cache that I can implement?
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There are 14 page offset bits. If 5 of them are used for block offset, there are 9 more that I can use for index.

512 sets ➔ 16KB direct-mapped or 32KB 2-way cache