

NITI MADAN

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AREAS OF INTEREST

Reliability-aware and power-efficient architectures, Performance analysis/power modeling of multi-core/many-core systems, 3D die stacking, Memory system design, Transactional memory

SUMMARY OF EXPERIENCE

- 6-months Post-silicon validation intern experience of Victoria Falls at Sun Microsystems
- 3 years research experience in Computer Architecture (Performance Analysis/modeling)
- 2 years research experience in Digital VLSI design (Asynchronous circuit design, FPGA based designs)
- 2 years experience as a teaching assistant for various CS/CE courses

EDUCATION

Aug'04-Present

Ph.D. in Computer Science

[University of Utah](#)

Current Overall G.P.A.: 3.9/4.00

Expected Graduation date: Aug 2009

Aug'01-Aug'04

M.S. in Computer Science

[University of Utah](#)

G.P.A.: 3.88/4.00

Aug'97-May'01

B.E. in Electrical Engineering

[Delhi College of Engineering](#)

University of Delhi, India

Marks Obtained: 73% (Not under GPA system)

RESEARCH EXPERIENCE

Jan'05- Present: Dissertation Research in Computer Architecture

Advisor: [Prof. Rajeev Balasubramonian](#), Assistant Professor, School of Computing, University of Utah

Dissertation: "*Efficient Mechanisms to Improve Processor Reliability*" – As a result of aggressive technology scaling, the error rates in a processor-- such as radiation-induced soft errors, hard errors and process variation-induced timing errors-- have increased significantly over the last few years. This has led to increased reliability support techniques in a processor such as redundant execution of a program. However, most of these solutions introduce performance loss and/or power cost due to the added redundancy. My dissertation research involves exploring efficient micro-architectural techniques to optimize power, performance and reliability in a processor. I am currently exploring designing error-tolerant hardware transactional memory protocols.

Following are contributions till date:

- Leveraging 3D die stacking technology for improving processor reliability by exploiting heterogeneous process for implementing redundant hardware (**MICRO-40**).
- Employing simple in-order checkers that can be frequency scaled for reducing power overheads of redundancy in chip-level redundant multithreading for single threaded and multi-programmed workloads (**TPDS'07**, SELSE-2).
- Improving register file reliability and reducing performance overheads in a redundantly threaded processor via eager register release (WAR-2).

May'02- Dec'03 : Research Assistant in Asynchronous Circuits and System Design Group
Advisor: [Prof. Erik Brunvand](#) , Associate Professor, School of Computing, University of Utah

- **Masters Thesis:** [“Asynchronous Microengines for Network Processing”](#)
Masters thesis research involved designing an Asynchronous Micro-programmable Network Processing Framework. Asynchronous circuit design was used to prototype this IP router on a Xilinx FPGA board. Extensions such as stateless firewalling etc. were added by modifying the microcode ([ANCHOR](#)).
- Explored a design methodology for implementing asynchronous circuits modeled with bundled-delays on Xilinx FPGAs.

June'00-Aug'00 : Intern at [Ministry of Information Technology](#), Microelectronics and Photonics Division , Center of VLSI Design and Prototyping, New Delhi, India
Worked on CAD tool design flow methodology for VHDL based designs using Synopsys tools.

REFEREED PUBLICATIONS

- [“Leveraging 3D Technology for Improving Processor Reliability”](#), Niti Madan and Rajeev Balasubramonian, *40th International Symposium on Microarchitecture 2007 (MICRO-40)*
- [“Power-efficient Approaches to Redundant Multithreading”](#), Niti Madan and Rajeev Balasubramonian, *IEEE Transactions on Parallel and Distributed Systems (TPDS), Special Issue on CMPs, August 2007*
- [“Exploiting Eager Register Release in a Redundantly Multi-Threaded Processor”](#), Niti Madan and Rajeev Balasubramonian, *2nd Workshop on Architectural Reliability (WAR-2) to be held in conjunction with MICRO-39 2006*
- [“A First-Order Analysis of Power Overheads of Redundant Multi-Threading”](#), Niti Madan, Rajeev Balasubramonian, *2nd Workshop on System Effects of Logic Soft Errors (SELSE-2), April 2006*
- [“A case for Asynchronous Microengines for Network Processing”](#), Niti Madan and Erik Brunvand, *Advanced Networking and Communications Hardware Workshop (ANCHOR 2004) held in conjunction with 31st Annual Symposium in Computer Architecture (ISCA 2004)*

NON-REFEREED PUBLICATIONS

- [“Scalable, Reliable, Power-efficient Communication for Hardware Transactional Memory”](#), Seth Pugsley, Manu Awasthi, Niti Madan, Naveen Muralimanohar and Rajeev Balasubramonian, *Technical Report UUCS-08-001, January 2008*
- [“Power-efficient Approaches to Reliability”](#), Niti Madan, Rajeev Balasubramonian,
- [“Asynchronous Microengines for Network Processing”](#), Niti Madan, *Masters Thesis, August 2004, University of Utah*

POSTER PRESENTATIONS

- “Power-efficient Approaches to Reliability”, Presented at *CRA-W and CDC Computer Architecture Summer School, Princeton University, July 2006*
- “Power-efficient Approaches to Reliability”, Presented at *Research Day, School of Computing, University of Utah, March 2005*

INDUSTRY EXPERIENCE

Feb'07-Aug'07: Post-Silicon Debug/Validation Intern at Sun Microsystems, Santa Clara, CA
Mentor: Ramaswamy Sivaramakrishnan, Principal Engineer
Assisted Root-cause analysis team in system-level post-silicon debug of the next generation Sun's processor “Victoria Falls”.

TEACHING/SCHOOL EXPERIENCE

- Teaching Assistant for [Engineering Programming](#) in Spring 2005
- Teaching Assistant for [Advanced I.C. Design](#) in Fall 2004
- Reference Library Aide in Science and Engineering Department at [Marriott Library, University of Utah](#) in Summer 2004
- Teaching Assistant for [Asynchronous VLSI Architecture](#) in Spring 2004
- Teaching Assistant for [Theory of Computation](#) in Spring 2002
- Teaching Assistant for [Computer Architecture](#) in Fall 2001

SKILL SET

- *Architecture Simulator* – SimpleScalar (Modified SimpleScalar to model a dual core SMT simulator)
- *Hotspot and Wattch* – Architecture-level Temperature and Power modeling
- *CMOS Digital Design and Asynchronous System Design*
- *Programming Languages* - C, VHDL, Matlab, Perl Scripting and also familiar with Verilog, Scheme, OCaml
- *Operating Systems* – Unix, Windows
- *CAD tools*- Synopsys VSS, Synopsys DC, Synopsys FPGA Compiler, Viewlogic (Powerview), Xilinx ISE, Cadence- Virtuoso Schematic Editor, Virtuoso Layout Editor, Analog Artist, VerilogXL, Silicon Ensemble, Modelsim
- *VLSI testing tools* – Hitec and Opus
- *Familiar with Verification Tool* - SPIN (using Promela)

COURSES TAKEN DURING M.S. AND Ph.D.

[Advanced I.C. Design I](#), [Advanced Computer Architecture](#), [Foundations of Computer Science](#), [Advanced I.C. Design II](#), [Programming languages and Semantics](#), [Operating System Design](#), [Async/Architecture Seminar](#), [Special topics in High Performance Architectures](#), [Computer Networks](#), [VLSI Testing and Verification](#), [Parallel Computer Architecture](#), [Research Proposals](#)

COURSE PROJECTS

- Design and layout of custom ASIC implementation of single-issue, dual-pipelined microprocessor based on National Semiconductor's CR-16A processor (Group project).
- Design and layout of 0.5 micron CMOS operational-amplifier using Cadence suite of tools. Awarded the *Best Student Design in High Speed Op-amp Design Category*.
- Implemented a type-checker for a given typed-lambda-calculus implementation in OCaml.
- Implemented a Unix-type Multi-threaded File-System in C using a simulated block device interface.
- Implemented a timer, sleep function, semaphores and proportional share scheduler for a user-level thread library package for Solaris in C.
- Implemented and verified mutual exclusion algorithms using SPIN and Promela. Team *won the 2nd place* in the OS course for writing the fastest and the most fair dining philosophers C code.
- Evaluated performance of heterogeneous clustered microarchitecture by steering critical instructions to high performance clusters and other instructions to low power clusters using SimpleScalar.
- Implemented a peer-to-peer Gnutella-like file sharing system for 3 peers in C using Socket programming.
- Implemented encryption/decryption application with the help of OpenSSL commands and Perl Scripting.
- Implemented an ATPG (Automatic test pattern generation) tool for detecting stuck-at faults in digital circuits using BDD package in VIS.

TALKS

Presented research work at workshops/conferences: ANCHOR-2004, SELSE-2, WAR-2, MICRO-2007

PROFESSIONAL MEMBERSHIP/OTHER SERVICES

- Student Member – IEEE, ACM, ACM-SIGARCH
- External Reviewer for Async'03, HPCA'07, IEEE TCAD'07
- Volunteer Treasurer for Non-profit Organization ASHA, Support-A-Child project, Silicon Valley Chapter

REFERENCES

Available upon request.