Mike Parker

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My primary focus is high-performance scalable system architecture. I have significant experience in numerous aspects of computer design, including processor architecture, network architecture, memory system architecture and I/O subsystems. My broad perspective of computer systems allows me to approach architecture from a low-level hardware perspective as well as from a high-level software, compiler, and operating systems perspective. I have strong background in the architecture and design of highly scalable shared-memory and message-passing systems, vector processors, threaded architectures, scalar microprocessors, memory systems, system network interfaces, and interconnection network architectures. I have experience in simulator development, architectural modeling and evaluation, as well as in application and OS porting and development.

Furthermore, I have substantial background in hardware design. I have designed non-trivial pieces of hardware using VHDL and Verilog at the behavioral, RTL and gate levels. I have experience with custom layout, standard cell design, spice, DRC, ERC, LVS and tape-out with CAD tools from multiple vendors. I have been involved in the architecture, design, and testing of semi-custom and standard cell chips across several CMOS technology generations. I have real world experience with synthesis, schematic entry, and board layout.

Professional Experience

- Cray, Inc., Sr. Architect, December 2003 – present

  Involved in development of "Cascade" (DARPA HPCS funded supercomputer system); Currently focused on adaptive routing, a table driven network routing architecture, and a high-radix router microarchitecture; Defined an efficient system network packet architecture; Architected a high-throughput DDR3 memory system; continuing investigation of future memory systems; Defined a global system memory addressing architecture; Defined functional unit pipeline microarchitecture; Worked on highly threaded and vector processor architectures enhancements; Given numerous government and customer presentations; Ongoing work with mechanical engineering group to optimize packaging of system architecture; Ongoing interaction a broad spectrum of engineers on issues related to hardware design, resilience, compiler, operating system, programming environment, technology, and packaging.
- University of Utah, School of Computing, Research Staff, June 1999 – December 2003

  SGI/DARPA HPCS Project (2002-2003)

  Evaluated the inclusion of Avalanche and Impulse project research ideas in SGI's proposed DARPA HPCS system; Along with the Utah team, worked with teams from SGI, MIT, UMN, and GWU to investigate performance, reliability, and programmability enhancements to large-scale commercial DSM systems.

  Impulse research project (1999-2002)

  Architected the Impulse memory controller; Led the hardware prototyping effort; Managed the hardware team of several M.S. and Ph.D. students; Designed pieces of the system, including the front-end to the scatter/gather address generator, the gather unit, and the I/O interfaces; Maintained commercial CAD tools, developed internal design tools, and played a significant role in the design and layout of Impulse system test boards; Significant in-lab testing of hardware.
- Phobos Corporation, VLSI and Hardware Engineer, August 1998 - June 1999

  Provided expertise necessary to migrate an FPGA-based Ethernet MAC into an ASIC; Developed prototype hardware (board and logic design) for a high-bandwidth network switch.
- University of Utah, School of Computing, Research Assistant, December 1995 - June 1999

  Avalanche and Impulse research projects

  Developed architectural simulators; Researched message cache architecture and microarchitecture; Designed and built a message-cache controller, a command queue, flash and I/O controllers, and test interfaces; Helped specify, design, and layout a fully custom FIFO, an SRAM, and I/O pads; Performed ASIC place and route, clock-tree generation, timing closure, and tape-out design checks; Developed tools to place logos on ASICs and to verify and debug designs; Design test PCBs; Developed OS & application code to test designs; Maintained commercial CAD tools.
- University of Utah, School of Computing, Teaching Assistant, Fundamentals of VLSI Design, September 1995 - December 1995

- University of Oklahoma, Department of Aerospace and Mechanical Engineering, Software Engineer / Systems Administrator, August 1992 - August 1995
- Consulting – System Administration and Software Development, YKS International, Dr. Ajay Agrawal, Dr. Sam Lee, Dr. Joe Bastian, and Dr. Ron Cox, 1993-1995
- University of Oklahoma, Department of Physics and Astronomy, Research Assistant, 1989 – 1990

Education

Ph.D. Candidate, University of Utah, Advisor Dr. Al Davis

Dissertation Title: *Efficient User-level Event Notification*

My dissertation focuses on reducing message-passing and I/O overhead by exposing interrupt-like notification mechanisms directly to the user. Specifically, I am improving the performance of fine-grained messages by avoiding OS overhead through a tightly coupled network interface and hardware based user-level thread wakeup mechanisms in an SMT processor.

Bachelor of Science in Electrical Engineering, University of Oklahoma. May 1995

Publications

- *Active Memory Operations*, Zhen Fang, Lixin Zhang, John Carter, Ali Ibrahim and Mike Parker, 21st International Conference on Supercomputing, 2007
- *The design and utility of the ML-RSIM system simulator*, Lambert Schaelicke, Michael Parker, Journal of Systems Architecture, Elsevier, vol 52(5), pp.283-297, 2006
- *ACT: A Low Power VLIW Cluster Coprocessor for DSP Applications*, Ali Ibrahim, Al Davis, and Mike Parker, ODES Workshop, in conjunction with CGO, 2006.
- *Efficient Address Remapping in Distributed Shared-Memory Systems*, Lixin Zhang, Mike Parker and John B Carter, ACM Trans. on Arch. and Code Optimization, Vol. 3, Issue 2, pp 209-229, June 2006.
- *Scalable Barriers for Large-scale Shared Memory Multiprocessors*, Zhen Fang, Lixin Zhang, John Carter and Mike Parker, International Journal of High Performance Computing and Networking, 2005
- *Fast Synchronization on Shared-Memory Multiprocessors: An Architectural Approach*, Zhen Fang, Lixin Zhang, Liqun Cheng, John Carter and Mike Parker, J. of Par. and Dist. Comp., Vol.65,2005
- *A Low Power Architecture for Embedded Perception*, Binu K. Mathew, Al Davis, Michael A. Parker, CASES, September 2004
- *Energy Efficient Cluster Co-Processors*, Ali Ibrahim, Mike Parker, and Al Davis, ICASSP, 2004
- *Evolving real-time systems using hierarchical scheduling and concurrency analysis*, John Regehr, Alastair Reid, Kirk Webb, Michael Parker, and Jay Lepreau, RTSS 2003, December 2003.
- *A Case for User-Level Interrupts*, Mike Parker, HPCA Work-In-Progress, February 2002
- Message-*Passing for the 21st Century: Integrating User-Level Networks with SMT*, Mike Parker, Al Davis, Wilson Hsieh, Work. on Multithreaded Execution, Architecture and Compilation, Dec. 2001
- *The Impulse Memory Controller*, Lixin Zhang, Zhen Fang, Mike Parker, Binu K. Mathew, Lambert Schaelicke, John B. Carter, Wilson C. Hsieh, and Sally A. McKee, IEEE ToC, November 2001
- *Impulse: Building a Smarter Memory Controller*, Carter, Hsieh, Stoller, Swanson, Zhang, Brunvand, Davis, Kuo, Kuramkote, Parker, Schaelicke, and Tateyama, HPCA-5, January 1999
- *Memory System Support for Irregular Applications*, J. Carter, W. Hsieh, M. Swanson, L. Zhang, A. Davis, M. Parker, L. Schaelicke, L. Stoller, and T. Tateyama, LCR'98, May 1998
- *Interactive Ray Tracing for Volume Visualization*, S. Parker, M. Parker. Y. Livnat, P.-P. Sloan, C. Hansen, and P. Shirley, IEEE Trans. on Visualization and Computer Graphics, July-September 1999
- *Interacting with Gigabyte Volume Datasets on the Origin 2000*, S. Parker, P. Shirley, Y. Livnat, C. Hansen, P.-P. Sloan, and M. Parker, The 41st Annual Cray User's Group Conference, 1999
- *Efficient Communication Mechanisms for Cluster Based Parallel Computing*, Al Davis, Mark Swanson, Mike Parker, CANPC, December 1996
- *ML-RSIM Reference Manual*, Lambert Schaelicke, Mike Parker, TR 02-10, U. of Notre Dame, 2002

References

Dr. Steve Scott, CTO Cray Inc.	stevescott@charter.net	715-726-4757
Dr. John Carter	retrac@us.ibm.com	512-286-5584
Scott Schroeder, Cray Inc.	schroede@cray.com	715-726-4870
Dr. Al Davis, Ph.D. Advisor	ald@cs.utah.edu	801-581-3991