[Biography of Lixin Zhang]

Dr. Lixin Zhang is currently a Professor and a Vice General Engineer at Institute of Computing Technology, Chinese Academy of Sciences. He is the founding director of the Center for Advanced Computer Systems. Dr. Zhang received his BS in Computer Science from Fudan University in 1993 and his PhD in Computer Science from the University of Utah in 2001. Dr. Zhang was a research associate from 1999 to 2001 and a post-doctoral research associate from 2001 and 2003, both at the University of Utah. He was a member of the Novel Systems Architecture group in the IBM Austin Research Lab from 2003 to 2010. He acted as the Lead Research Advisor in the system & software area in the IBM Austin Center for Advanced Studies from 2005 to 2006.

Dr. Zhang has 20+ years of research experience in the areas of computer architecture, including high performance computing, microprocessor, memory systems, data center computing, and parallel/distributed computing. He was a chief performance architect and a lead co-designer of IBM's PERCS project and the (planned) supercomputer Blue Waters before he left IBM (The Blue Waters project was cancelled in Aug. 2011). Dr. Zhang has led the development of three cycle accurate full-system simulators and played leading roles in the design of two intelligent memory systems. He was a key member of the IBM Power7-IH team and participated in the development of the Cell processor. In addition to technical responsibility, Dr. Zhang has also enjoyed the responsibility of helping and advising junior group members in the various projects that he had been a technical leader.

Dr. Zhang has published over 50 scientific articles on peer-reviewed premium conferences and journals and filed over 100 patent applications. His work has been cited over 1000 times (according to Google Scholar). He has served more than forty times on conference organizing committees, government review panels, and editorial boards. He has received multiple awards from inside and outside IBM. Mostly recently, he won two Outstanding Technical Achievement Awards, three Technical Group Awards, three Bravo Awards, and eighteen Thanks! Awards from IBM. Dr. Zhang was a Master Inventor of IBM.

CURRICULUM VITAE *of*

Lixin Zhang

RESEARCH INTERESTS

Computer architecture, data center computing, advanced cache/memory systems, architectural simulators, distributed/parallel computing, performance evaluation, and workload characterization.

EDUCATION

- Ph.D. (Computer Science), University of Utah, 12/2001
  - *Dissertation*: Efficient Remapping Mechanisms for An Adaptable Memory System
- M.S. (Computer Science), Fudan University, 07/1995
- B.S. (Computer Science), Fudan University, 07/1993

WORK EXPERIENCE

- **Quick Index:**
  - 08.2010 – Present: Professor, Institute of Computing Technology, Chinese Academy of Sciences
  - 09.2003 – 08.2010: Research Staff Member & Lead Research Advisor, IBM Research
  - 01.2002 – 08.2003: Postdoctoral Research Associate, University of Utah
  - 07.1999 – 12.2001: Research Staff Member, University of Utah.
  - 01.1996 – 06.1999: Research Assistant, University of Utah
  - 09.1995 – 12.1995: Teaching Assistant, University of Utah
  - 07.1994 – 07.1995: Software engineer, Kingstar Computer Co.
  - 09.1991 – 07.1994: Research Assistant, Fudan University

1. **08.2010 – Present: Professor, Vice General Engineer, Institute of Computing Technology, CAS**

   Director, Advanced Computer Systems Laboratory

   - I lead the Advanced Computer Systems Laboratory. My team is currently exploring new ways to build the next-generation data center servers. We are looking for opportunities across the entire hardware and software stack, including ISAs and CPUs, chip/memory/storage/network architectures, system software, run-time environment, data center management systems, etc.

2. **09.2003 – 08.2010: Research Staff Member, IBM Austin Research Lab.**
   - **UHPC** (Ubiquitous High Performance Computing). I helped write the project proposal as the Chief Chip Architect. I was responsible for initial chip microarchitecture of the proposed UHPC processor. (The proposal was rejected with the following message in the rejection letter, the proposal ranked on the top technically, but …)
   - **PERCS** (Productive, Easy to use, Reliable Computer Systems). The goal of PERCS is to deliver a multi-petaflop high performance computer. As a key member of the architecture/performance team, I led or co-led the design and evaluation of various CMP cache memory hierarchies, including advanced cache coherence protocols, intra-chip cache communication topology, near memory processing, high performance memory hubs, memory in processor, and advanced data prefetching mechanisms. I also led the development of the PERCS simulator and developed its cycle accurate processor and nest models. I am a lead performance architect of the 10 Petaflops machine Blue Waters, initially scheduled to come out in 2011, but later cancelled by IBM.
   - **Power7,** I led the development of a cycle-accurate model in a full-system simulation environment

for the Power7 microprocessor. The model was about two orders of magnitude faster than IBM's existing simulator used by the product team at that time with comparable accuracy. I, working with the Chief Architects and other members in the research team and the development team, used this model to (i) to refine designs of various units in Power7, (ii) to push research ideas into the Power7, and (iii) to perform competitive analysis.

- **TRIPS** (Tera-op, Reliable, Intelligently adaptive Processing System). I studied various NUCA (non-uniform cache architecture) organizations for flexible CMP cache sharing mechanisms.
- **STI (a.k.a., Cell).** I developed cycle-accurate simulator models for the on-chip interconnect bus, cache coherence engine, and memory system of the Cell architecture. I also provided consulting services to its simulator development team.
- **ACAS** (IBM Austin Center for Advanced Studies). I was the **Lead Research Advisor** in the system & software area. I was responsible for reviewing/ranking proposals for IBM faculty awards and PhD fellowship awards and helping organize semi-annual CAS conferences.

3. **01.2002 – 08.2003: Postdoctoral Research Associate, University of Utah**.
I was a university partner of SGI's Ultraviolet project, whose goal was to design, evaluate, and produce peta-scale systems.

   - I led the design of Active Memory Systems, which exploited the potential and feasibility of incorporating processing power into the memory controllers.
   - I led the development of the simulator infrastructure used by the entire Ultraviolet team, which included researchers at SGI, MIT, George Washington University, and University of Utah.
   - I led the design of scalable coherence mechanisms and scalable synchronization mechanisms for large-scale CC NUMA systems.
   - I acted as the technical leader for a team of three graduate students and one undergraduate student.

4. **07.1999 – 12.2001: Research Associate, University of Utah**
As a full-time staff member of the Impulse Adaptable Memory Systems project, I played a leading role in the design/evaluation phase and a key role at the development phase. Overall, I had been a major contributor to

   - the architecture-level design,
   - simulator development,
   - kernel extension,
   - application analyses and performance evaluation, and
   - chip-level functional verification of the ASIC design.

5. **07.1996 – 07.1999: Research Assistant, University of Utah**
This was for my dissertation work. The key idea was to use an intelligent memory system to significantly increase the performance of the processor caches and the system bus by allowing applications to control how data should be present to the caches during runtime. For instance, multiple sparsely store data items in the memory may be merged a dense line in a cache.

- **04.1996 – 12.1996: Research Assistant** for project Avalanche Scalable Parallel Processor, **University of Utah**
Avalanche entailed the design and construction of a usable and scalable parallel computing platform that was not exorbitantly expensive, yet still capable of achieving high performance. My work was to design, simulate, and evaluate an assist cache and a hardware-directed cache prefetching mechanism.
- **01.1996 – 04.1996: Research Assistant** for project Module Manipulation, **University of Utah**
Worked as a programmer for this project, which added modularity to existing languages by providing a suite of operators that accept modules as arguments and produce modules as results.

- **09.1995 – 12.1995: Teaching Assistant** for class Digital System Design, **University of Utah**
  Grader and lab tutor for this undergraduate-level class about the fundamental concepts of digital system theory and design.
- **07.1994 – 07.1995: Software engineer**, Kingstar Computer Co., **P.R.China**
  Project manager and main developer of a four-member team to build a LAN-based system that traces manufacturing information in real time and generates instant feedbacks.
- **09.1991 – 07.1994: Research Assistant** for project **"***Remote Procedure Call", **Fudan University***
  Primary programmer of a project to implement the remote procedure call paradigm in a special environment.
- **09.1991 – 07.1993: Research Assistant** for project **"***OSI High Level Protocol Implementation Based On TCP/UDP/IP*", **Fudan University**
  Principal designer and programmer of an effort to implement the transport layer of the ISO/OSI model based on the TCP/UDP/IP implementation.

PUBLICATIONS

Journal Papers

- **The Implications of Diverse Applications and Scalable Data Sets in Benchmarking Big Data Systems**
  Zhen Jia, Lei wang, Wanling Gao, Yingjie Shi, Jianfeng Zhan, and Lixin Zhang**.**
  Lecture Notes in Computer Science, Jan 2014
- **CloudRank-D : Benchmarking and Ranking Cloud Computing Systems For Data Processing Applications**
  Chunjie Luo , Jianfeng Zhan , Zhen Jia , LeiWang , Gang Lu , Lixin Zhang , Cheng-Zhong Xu , Ninghui Sun.
  Frontiers of Computer Science, Vol. 6, No. 4, pp 347-362, Aug 2012.
- **海云计算实验系统研究**
  詹剑锋, 明子鉴, 王磊, 徐俊刚, 陈兴振, 张峰, 张立新, 孙凝晖
  《网络新媒体技术》, 2012 年 6 月 第一卷第 6 期
- **可重塑处理器：用户可定义的加速器中处理器架构**
  张磊, 王颖, 陈云霁, 徐志伟, 张立新
  《网络新媒体技术》， 2012 年 6 月 第一卷第 6 期
- **微服务器研究现状综述**
  王聪， 侯锐， 张立新
  《信息技术快报》 2012 年第 10 卷第 4 期
- **数据中心全系统模拟方法研究**
  胡农达， 付斌章， 隋秀峰， **李龙**， 朱晓东， 李涛， 陈明宇， 张立新
  《信息技术快报》 2012 年第 10 卷第 4 期
- **PERCS System Architecture.**
  E. N. Elnozahy, Evan Speight, Jian Li, Ramakrishnan Rajamony, Lixin Zhang and L. Baba Arimilli**.**
  Encyclopedia of Parallel Computing, Sept. 2011
- **Design Exploration of Hybrid cache architecture with disparate memory technologies.**
  Xiaoxia Wu, Jian Li, Lixin Zhang, Evan Speight, Ram Rajamony and Yuan Xie**.**
  ACM Transaction on Architecture and Code Optimization (TACO), Dec 2010
- **A NUCA Substrate for Flexible CMP Cache Sharing**

Jaehyuk Huh, Changkyu Kim, Hazim Shafi, Lixin Zhang, Doug Burger and Stephen W. Keckler.
Journal of IEEE Transactions on Parallel And Distributed Systems, Vol. 18, No. 8, pp 1028-1040, Aug 2007.

- **Efficient Address Remapping in Distributed Shared-Memory Systems**
  Lixin Zhang, Mike Parker and John B Carter.
  Journal of ACM Transactions on Architecture and Code Optimization, Vol. 3, Issue 2, pp 209-229, June 2006.
- **Application of Full-System Simulation in Exploratory System Design and Development**
  J.L. Peterson, P.J. Bohrer, E.N. Elnozahy, A. Gheith, R.H. Jewell, M.D. Kistler, T.R. Maeurer, S.A. Malone, D.B. Murrell, N. Needel, K. Rajamani, M.A. Rinaldi, R.O. Simpson, K. Sudeep, Lixin Zhang.
  IBM *Journal of Research and Development*, Vol. 50, No. 2/3,, pp. 321-333, 2006.
- **Fast Synchronization on Shared-Memory Multiprocessors: An Architectural Approach**
  Zhen Fang, Lixin Zhang, Liqun Cheng, John B Carter and Mike Parker.
  Journal of Parallel and Distributed Computing, 2005.
- **Scalable Barriers for Large-scale Shared Memory Multiprocessors**
  Zhen Fang, Lixin Zhang, John B Carter and Mike Parker.
  International Journal of High Performance Computing and Networking, Vol. 6 2004.
- **Mambo -- A Full System Simulator for the PowerPC Architecture**
  P. Bohrer, M. Elnozahy, A. Gheith, C. Lefurgy, T. Nakra, J. Peterson. R. Rajamony, R. Rockhold, H. Shafi, R. Simpson, E. Speight, K. Sudeep, E. Van Hensbergen, and L. Zhang.
  ACM SIGMETRICS Performance Evaluation Review, Volume 31, Number 4, March 2004
- **The Impulse Memory Controller**
  Lixin Zhang, Zhen Fang, Mike Parker, Binu Mathew, Lambert Schaelicke, John B Carter, Wilson C Hsieh, and Sally A McKee.
  Transactions on Computers, Vol 50, No. 11, pp 1117-1132, November 2001.
- **Impulse: Memory System Support for Scientific Applications**
  John B Carter, Wilson C Hsieh, Leigh Stoller, Mark Swanson, Lixin Zhang, and Sally A McKee.
  Journal of Scientific Programming, Vol 7, No 3-4, pp. 195-209, 1999.
- **Transition from TCP/IP to OSI protocol**
  Lixin Zhang, Zhaodong Cui, and Chuanshan Gao.
  Journal of Computer Applications and Software (ISSN 1000-386X), Vol. 12, No. 2, pp. 1-7, 1995.
- **RPC and Its implementation in UNIX Environment**
  Chuanshan Gao, Bo Wu, Lixin Zhang, and Xiangyang Chen.
  Computer Engineering Journal (ISSN 1000-3428), Vol.19, No.5, pp. 37-42, 1993.

Refereed Conference and Workshop Papers

- **Rethinking Virtual Machine Interference in the Era of Cloud Applications**
  Tianni Xu, Xiufeng Sui, Zhicheng Yao, Jiuyue Ma, Yungang Bao, Lixin Zhang
  In the *Proceedings of 15th IEEE International Conference on High Performance Computing and Communications, Nov, 2013.*
- **A High-Performance and Cost-Efficient Interconnection Network for High-Density Servers**
  Wentao Bao, Binzhang Fu, Mingyu Chen and Lixin Zhang.
  In the *proceedings of 15th IEEE International Conference on High Performance Computing and Communications, Nov, 2013.*
- **Nimble: A Fast Flow Scheduling Strategy for OpenFlow Networks**
  Long Li, Binzhang Fu, Mingyu Chen and Lixin Zhang
  HPC-China 2013

- **Characterizing Data Analysis Workloads in Data Centers**
  Zhen Jia, Lei wang, Jianfeng Zhan, Lixin Zhang and Chunjie Luo
  In the *Proceedings of 2013 IEEE International Symposium on Workload Characterization, Sep 2013.*
- **ACSim：一个面向 ARMv8 体系结构的处理器仿真平台**
  江涛，张乾龙，张义，张乐乐，柴琳，韩晶，张武香，王聪，侯锐，张立新，孙凝晖
  第十七届计算机工程与工艺年会暨第三届微处理器技术论坛论文集，2013. 07. 20
- **并行模拟技术研究**
  江涛； 隋秀峰； 张立新； 侯锐； 李龙； 霍志刚； 赵晓芳；孙凝晖
  第十五届计算机工程与工艺年会暨第一届微处理器技术论坛论文集，2013. 07. 20
- **Characterizing OS behavior of Scale-out Data Center Workloads**
  Chen Zheng, Jianfeng Zhan, Zhen Jia, and Lixin Zhang.
  Seventh Annual Workshop on the Interaction amongst Virtualization, Operating Systems and Computer Architecture，in conjunction with ISCA2013, Jun, 2013.
- **DCNSim: A Unified and Cross-layer Computer Architecture Simulation Framework for Data Center Network Research**
  Nongda Hu, Binzhang Fu, Xiufeng Sui, Long Li, Tao Li, and Lixin Zhang.
  In the *Proceedings of ACM International Conference on Computing Frontiers, May, 2013.*
- **Understanding the Implications of Virtual Machine Management on Processor Microarchitecture Design**
  Xiufeng Sui, Tao Sun, Tao Li, Lixin Zhang, Zilong Wang
  In the *Proceedings of 2013 IEEE International Symposium on Performance Analysis of Systems and Software, Apr, 2013.*
- **Micro-architectural Characterization of Desktop Cloud Workloads**
  Tao Jiang, Rui Hou, Lixin Zhang, Ke Zhang, Licheng Chen, Mingyu Chen and Ninghui Sun.
  In the *proceedings of IEEE International Symposium on Workload Characterization, Nov, 2012*
- **High Volume Throughput Computing: Identifying and Characterizing Throughput Oriented Workloads in Data Centers**
  Jianfeng Zhan, Lixin Zhang, Ninghui Sun, Lei Wang, Zhen Jia, and Chunjie Luo,
  Workshop on Large-Scale Parallel Processing in conjunction with 26th IEEE International Parallel and Distributed Processing Symposium, Shanghai, China, May, 2012
- **Characterization of Real Workloads of Web Search Engines**
  Huafeng Xi, Jianfeng Zhan, Zhen Jia, Xuehai Hong, Lixin Zhang and Ninhui Sun
  In the Proceedings of IEEE International Symposium on Workload Characterization, Nov., 2011
- **Application-driven Energy-efficient Architecture Explorations for Big Data**
  Xiaoyan Gu, Rui Hou, Ke Zhang, Lixin Zhang and Weiping Wang
  In the Proceedings of The First Workshop on Architectures and Systems for Big Data, Oct., 2011
- **Adapt or Become Extinct!**
  G. Goumas, S. A. McKee, M. Själander**,** T. R. Gross, S. Karlsson, and L. Zhang
  In the *Proceedings of IEEE Workshop on Adaptive Self-Tuning Computing Systems for the Exaflop Era*, Jun. 2011
- **Enigma: Architectural And Operating System Support for Reducing The Impact of Address Translation**
  L. Zhang, E. Speight, R. Rajamony, J. Lin
  In the *Proceedings of ACM IEEE International Conference on Supercomputing*, Jun. 2010

- **Power Shifting in Thrifty Interconnection Network**
  Jian Li, Lixin Zhang, Wei Huang, Charles Lefurgy, Wolfgang Denzel, Richard Treumann, Kun Wang
  In the *Proceedings of International Symposium on High Performance Computer Architecture*, Feb., 2010.
- **Efficient Data Streaming with On-chip Accelerators: Opportunities and Challenges**
  Rui Hou, Lixin Zhang, Michael C Huang; Kun Wang, Hubertus Franke, Yi Ge, Xiao Tao Chang
  In the *Proceedings of International Symposium on High Performance Computer Architecture*, Feb., 2010.
- **Thrifty Interconnection Networks for HPC systems**
  Jian Li, Lixin Zhang, Charles Lefurgy
  Abstract in *proceedings of ACM International Conference on Supercomputing*, New York, June, 2009.
- **Power and Performance of Read-Write Aware Hybrid Caches**
  Xiaoxia Wu, Jian Li, Evan Speight, Lixin Zhang and Yuan Xie,
  In *Design, Automation & Test in Europe (**DATE**) 2009*, Nice, France, April 20-24, 2009
- **Power and performance evaluation for 3D hybrid cache with non-volatile memory**
  Xiaoxia Wu, Jian Li, Lixin Zhang, Evan Speight and Yuan Xie,
  In ***HPCA*** 3D Workshop, Raleigh, North Carolina- February 15, 2009
- **Light-weight predication support in OOO superscalar processors**
  Mark Stephenson,, Lixin Zhang, and Ram Rangan
  In the *Proceedings of International Symposium on High Performance Computer Architecture*, Feb. *HPCA'2009*
- **Active Memory Operations**
  Zhen Fang, Lixin Zhang, John Carter, Ali Ibrahim and Mike Parker.
  In the *Proceedings of the 21st International Conference on Supercomputing*, June 2007
- **A NUCA Substrate for Flexible CMP Cache Sharing**
  Jaehyuk Huh, Changkyu Kim , Hazim Shafi, Lixin Zhang, Doug Burger, and Stephen W. Keckler.
  In the *Proceedings of the 19th ACM International Conference on Supercomputing*, June 2005
- **Adaptive Mechanisms and Policies for Managing Cache Hierarchies in Chip Multiprocessors**
  Evan Speight, Hazim Shafi, Lixin Zhang, and Ram Rajamony
  In the *Proceedings of the 32nd Annual International Symposium on Computer Architecture*, Madison, Wisconsin, June 2005.
- **Highly Efficient Synchronization Based on Active Memory Operations**
  Lixin Zhang, Zhen Fang and John B Carter.
  In the *Proceedings of the International Parallel and Distributed Processing Symposium*, April 2004
- **Super-Fast Active Memory Operations-Based Synchronization**
  Lixin Zhang, Zhen Fang, John B. Carter, and Mike Parker
  The 2nd Workshop on Hardware/Software Support for High Performance Scientific and Engineering Computing, September 2003.
- **Reevaluating Online Superpage Promotion with Hardware Support**
  Zhen Fang, Lixin Zhang, John B Carter, Sally A McKee, Wilson C Hsieh.
  In the *Proceedings of the Seventh International Symposium on High Performance Computer Architecture* , pp. 63-72, January 2001
- **Memory System Support for Dynamic Cacheline Assembly**
  Lixin Zhang, Venkata K Pingali, Bharat Chandramouli, and John B Carter.
  In the *2nd Workshop on Intelligent Memory Systems*, August, 2000.

- **Pointer-Based Prefetching within the Impulse Adaptable Memory Controller: Initial Results**
  Lixin Zhang, Sally A McKee, Wilson C Hsieh, and John B. Carter.
  In the *ISCA-2000 Workshop on Solving the Memory Wall Problem*, June 2000.
- **Online Superpage Promotion Revisited**
  Zhen Fang, Lixin Zhang, John B Carter, Sally A McKee, and Wilson C Hsieh.
  In the *Proceedings of SIGMETRICS 2000 International Conference on Measurement and Modeling of Computer Systems*, June 2000.
- **Memory System Support for Image Processing**
  Lixin Zhang, John B Carter, Wilson C Hsieh, and Sally A. McKee.
  In the *Proceedings of International Conference on Parallel Architectures and Compilation Techniques (1999)*, pp. 98-107, October 1999.
- **Impulse: Building a Smarter Memory Controller**
  John Carter, Wilson Hsieh, Leigh Stoller, Mark Swanson, Lixin Zhang, Erik Brunvand, Al Davis, Chen-Chi Kuo, Ravi Kuramkote, Mike Parker, Lambert Schaelicke, and Tera Tateyama.
  In the *Proceedings of Fifth International Symposium on High Performance Computer Architecture*, pp. 70-79, January 1999.
- **Memory System Support for Irregular Applications**
  John Carter, Wilson Hsieh, Mark Swanson, Lixin Zhang, Al Davis, Mike Parker, Lambert Schaelicke, Leigh Stoller, and Tera Tateyama.
  In the *Fourth Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers* , pp. 9-14, May 1998

Technical Reports

- **Developers Manual of Mambo's Cycle Accurate Core Model**
  Lixin Zhang.
  IBM Confidential, February, 2009.
- **How to Develop Mambo Source Code**
  James Peterson, Lixin Zhang.
  IBM Confidential, March, 2008.
- **Reference Manual of Mambo's Bus Model**
  Lixin Zhang.
  IBM Confidential, May, 2006
- **URSIM User Manual**
  Lixin Zhang.
  Technical report UUCS-03-011, University of Utah, March, 2003.
- **Functionality of the Impulse Memory Controller**
  Lixin Zhang.
  Technical report UUCS-01-009, University of Utah, July, 2001.
- **URSIM Reference Manual**
  Lixin Zhang.
  Technical report UUCS-00-015, University of Utah, August, 2000.
- **A DRAM Backend for The Impulse Memory System**
  Lixin Zhang.
  Technical report UUCS-00-002, University of Utah, January, 2000.
- **A Comparison of Online Superpage Promotion Mechanisms**
  Zhen Fang and Lixin Zhang.
  Technical report UUCS-99-021, University of Utah, December, 1999.
- **Reference Manual of Impulse System Calls**
  Lixin Zhang and Leigh Stoller.

Technical report UUCS-99-018, University of Utah, October, 1999.

- **ISIM: The Simulator for The Impulse Adaptable Memory System**
  Lixin Zhang.
  Technical report UUCS-99-017, University of Utah, September, 1999.

PROFESSIONAL SERVICES

1. Program committee member, The 41st International Symposium on Computer Architecture, June 2014
2. Program committee member, International Symposium on High Performance Computer Architecture (HPCA'2015), Feb. 2015
3. Steering committee member, International Symposium on High Performance Computer Architecture (HPCA'2015), Feb. 2015
4. Program committee co-Chair, IEEE International Symposium on Workload Characterization, October 2014
5. Program committee member, IFIP International Conference on Network and Parallel Computing (NPC'2014), Sept. 2014
6. External Program committee member, International Conference on Parallel Architectures and Compilation Techniques, 2014
7. Co-chair for the architecture track, International Conference on Network, Architecture, and Storage, 2014
8. Program committee member, The 41st International Symposium on Computer Architecture, June 2014
9. General co-Chair, Fourth Workshop on Architectures and Systems for Big Data (ASBD 2014), June 2014
10. Program committee member, The Memory Forum, June 2014
11. Steering committee member, International Symposium on High Performance Computer Architecture (HPCA'2014), Feb. 2014
12. General co-Chair, 10th IFIP International Conference on Network and Parallel Computing (NPC'2013), Sept. 2013
13. Program committee member, The 17th CCF Annual Conference on Computer Engineering and Technology, July 2013
14. Program committee co-Chair, Third Workshop on Architectures and Systems for Big Data (ASBD 2013), June 2013
15. Technical program committee member, The International Symposium on Low Power Electronics and Design (ISLPED), June 2013
16. General Chair, The 19th International Symposium on High Performance Computer Architecture (HPCA'2013), Feb. 2013
17. Board of Distinguished Reviewers, the International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC), 2013, 2014
18. General Chair, ACM SIGPLAN Workshop on Memory Systems Performance and Correctness, June 2012
19. Program committee co-chair, Workshop on Large-Scale Parallel Processing, May 2012
20. Program committee member, 26th IEEE International Parallel & Distributed Processing Symposium, May 2012, 2014
21. Workshops and Tutorials co-Chair, The 18th International Symposium on High Performance Computer Architecture, Feb., 2012
22. Program committee member, IEEE International Conference on Supercomputing, 2011, 2013,2014
23. Program committee member, IEEE Asia-Pacific Services Computing Conference (IEEE APSCC), 2008, 2009
24. Program Committee member, 3rd International Symposium on Trustworthiness, Reliability and services in Ubiquitous and Sensor neTworks (TRUST-08), Dec. 2008
25. International Editorial Board, Special Issue of AutoSoft Journal "Applications and Security Services in Web and Pervasive environments", 2008
26. Program Committee, Wuhan International Conference on E-Business, 2008, 2009
27. Financial chair, International Symposium on high performance computer architecture (HPCA'08), Feb 2008

28. Program committee member, The 2007 Asia-Pacific Services Computing Conference (APSCC-07), December 2007
29. Program committee member, International Conference on high performance computing, networking and storage (SC07), Nov. 2007
30. Program committee member, International Conference on Network and Parallel Computing, 2007, 2011
31. Program committee member, Workshop on the Interaction between Operating Systems and Computer Architecture, June 2007
32. Financial chair, International Conference on Parallel Architectures and Compilation Techniques, September 2006
33. Program committee member, International Conference on Parallel Processing, August 2006
34. Program committee member, IBM 7th Annual Austin Center for Advanced Studies Conference, February 2006
35. Co-chair, program committee member, Workshop on Memory Performance Issues, February 2006
36. Session chair, IEEE International Symposium on Workload Characterization, October 2005
37. Program committee member, International Conference on Network and Parallel Computing, November 2005
38. Program committee member, IBM 6th Annual Austin Center for Advanced Studies Conference, February 2005
39. Co-chair, program committee member, Workshop on Memory Performance Issues, June 2004
40. Panelist, NSF Computer System Architecture Review Panel, May 2004
41. Submission chair, International Conference on Parallel Architectures and Compilation Techniques, September 2003
42. Session chair, International Conference on Parallel Architectures and Compilation Techniques, September 2002
43. Web chair, International Conference on Parallel Architectures and Compilation Techniques, September 2002

PROFESSIONAL MEMBERSHIPS

- Senior Member of ACM
- Senior Member of IEEE

AWARDS

- IBM, Master Inventor, 2009
- IBM, Equity Award, "*To recognize your critical contribution to IBM's success*", Nov. 2009
- IBM, Bravo Award, "*Assistance with SMT tracing for P7 verification*", July. 2008
- IBM, Outstanding Technical Achievement Award, "*Demonstration of IBM's Leadership in HPC through PERCS*", Mar. 2008
- IBM, Bravo Award, "*Contributions to closing the NCSA deal and the supporting performance work*", Nov. 2007
- IBM, Retention Award, "*In recognition of your skills and anticipated contributions and your critical role*", July, 2007
- IBM, Outstanding Technical Achievement Award, "*Core Contributions to the success of the Mambo Full System Simulator*", Jan. 2007
- IBM, Bravo Award, "*Delivering the force behind: PlayStation 3*", Dec. 2006
- IBM, Research Division Technical Group Award for "*Contributions to the success of PERCS Milestone 6*", March, 2006
- IBM, Research Division Team Group Award for "*Delivery of IBM's Full System Simulator for Cell Broadband Engine as part of the Cell SDK 1.0 Global Release*", December, 2005

- IBM, Research Division Technical Group Award for "*IBM Full System Simulator (Mambo) Public Cell Release and Impact on Xbox 360 Product Release*", December, 2005
- IBM, Invention Achievement Award, February, 2005
- Graduate Research Supplement Award, University of Utah, June, 2000
- Conference Travel Grant: HPCA-2001, ASPLOS-2000, PACT-99, and HPCA-99
- Excellent Graduate Award, Fudan University, July, 1993
- People's Scholarship, Fudan University, every semester during 09/1989 -- 07/1993

PATENTS (Granted)

1. US8739159, "Cache partitioning with a partition table to effect allocation of shared cache to virtual machines in virtualized environments", Jiang Lin, Lixin Zhang
2. US8612691, "Assigning Memory To On-Chip Coherence Domains", William Speight, Lixin Zhang
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