VLSI Logic Test, Validation and Verification

Efficient Test methodologies for SOC Cores and Interconnects
Looking at the future?

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Problem Statement:

Improvements in process technology have resulted in dramatic increases in clock speeds and transistor budgets. Entire systems can now be implemented on a single chip (SoCs). However, Interconnects do not scale as well as their transistor counterparts. Empirical Studies have shown that power dissipation associated with long interconnects accounts for a significant fraction of the total power dissipated by the chip. Thus, Interconnects are becoming critical determinants for Performance, Reliability and Power. Test methodologies that look at these orthogonal constraints while maintaining maximum fault coverage have not been studied well. However, with the rapid emergence of SoCs and embedded cores, this problem need to be addressed.

In this study, we propose to analyze some existing test methodologies for logic cores and interconnects. The final goal is to identify a low power, high speed test methodology that can test these cores and interconnects with maximum fault coverage.

Introduction:

As process technology shrinks and clock frequency increases, cross-coupling effects between circuit components leads to significant crosstalk problems that are becoming too critical to be ignored. The fact that supply voltage decreases as we go to deep sub-micron technologies exacerbates this problem. Accurate analysis and realizable test methods for these cores and interconnects are a necessity to ensure the reliability and functionality of future SoCs.

Addressing the problem of crosstalk at the process level is too involved and prohibitive. To mitigate this problem, researchers use abstract fault models to represent all crosstalk defects with a small number of faults. The Maximal Aggressor Fault Model (MAFM) [4] represents all the process variations and physical defects as one of the following crosstalk errors: positive glitch, negative glitch, rising delay and falling delay. The problem now arises from the fact that we would like to implement methodologies that can test both the logic and the interconnects efficiently. In an attempt to realize this, we plan to extend existing techniques used for testing cores to encompass crosstalk faults. LI-BIST [3], (Logic-Interconnect Built In Self Test) is one such comprehensive self-test solution for both the logic and interconnects of SoCs. This method reuses existing logic BIST structures to reduce power consumption and the area overhead.
Project Deliverables:

The first step in this project is to thoroughly analyze existing test methodologies ([1], [2], [3]). Identifying limitations in existing techniques will be the next step. Our final step is to propose a new method that overcomes these limitations. As part of future work, we would also like to focus on future problems that influence these methodologies.

References:


