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EDUCATION

- Ph.D. and M.S. degree in the Dept. of Electrical and Computer Engineering
  University of Utah expected spring 2003
- B.S. degree in the Dept. of Computer Science
  University of Utah December 1997
- 5-year college degree in the Dept. of Electronics
  South Taiwan University of Technology (Former Nan-Tai College) May 1990

Title: *Intelligent Security System for A Small Community*

Advisors: Associate Professor Jin-Liang-Yang

DISSERTATION

Title: *Transistor-level Technology Mapping for Generalized C-element (gC) Implementation of XBM Controller*

Topics: Technology Mapping, Asynchronous Circuit Design, CAD Algorithms, Dynamic Logic, and Self-Timed Datapath Component

Advisors: Associate Professor Erik Brunvand
Professor Ganesh Gopalakrishnan

Abstract:

In this research, I developed a transistor-level technology mapping technique for multiple input change (MIC) fundamental mode asynchronous controllers. The major contribution of this work is a pre-layout technology mapper and a design methodology to utilize it for asynchronous VLSI design. This technology mapper takes a set of synthesized raw generalized C-element (gC) equations and environment specifications in either burst-mode (BM) or extended BM (XBM) format. Transition probabilities are extracted from the given environment specification for optimization and hazard-preserving transformation purpose. The gC equations are then mapped into a transistor network for the target CMOS technology. All transistors in the mapped network are sized either by designers or my automatic sizing procedure based on optimization cost metrics. This technology mapper does not make any assumption for the gC implementation and controller specifications, any high-level BM/XBM synthesis tool can be used to generate technology independent raw gC equations needed. The pre-layout optimization strategies explored in this research can also be adopted to improve bundled-data delay self-timed datapath components.

RELEVENT RESEARCH WORK

Title: *Self-Timed Design with Dynamic Circuits*

Abstract:

We introduce a simple hierarchical design technique for building high-performance self-timed components using dynamic domino-style circuits. This technique is useful for building handshaking style functional blocks and for self-timed data path components. We wrap the dynamic domino circuit in a wrapper that communicates using a req/ack protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. The circuit overhead required for this early-acknowledge feature is relatively small, but can provide measurable speedup in some situations. We call this approach semi-bundled delay (SBD). SBD wrapped circuits allow a designer to take advantage of high-speed dynamic data path circuits that can be used with any self-timed or asynchronous design style that relies on an explicit completion acknowledge signal.

Title: *Semi-Bundled Wrappers for Self-Timed Dynamic Domino Circuits*

Abstract:

We introduce a simple hierarchical design technique for using dynamic domino circuits to build high-performance self-timed data path circuits. We wrap the dynamic domino circuit in a wrapper that communicates using a re-quest/acknowledge protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. We call the resulting wrapper semi-bundled because of this early acknowledge. The circuit overhead required for this semi-bundled feature is relatively small, but can provide measurable speedup in some situations. The technique is suitable for any dynamic logic family that has a pre-charge/evaluate cycle, and that produces monotonic output transitions.

Title: *Extended Burst-Mode (XBM) Asynchronous FSM (AFSM) Reshuffling*

Abstract:

I defined a set of rules to move XBM transition signals either to its previous state(s) or subsequent state(s) without altering the transition properties. By doing so, some states become empty and can be removed to simplify the controller design. I developed a tool called XBM Reshuffler to automate this reshuffling procedure. This tool is built to optimize synthesized XBM controllers from ACK (a framework for high level synthesis of Asynchronous circuits that developed in the University of Utah). Since, XBM Reshuffler is a high level and technology independent XBM AFSM optimization tool, all targeting VLSI technologies (FPGA, CMOS, SOI, and etc.) can benefit from it. For all the sample circuits I tested, approximately 15% to 20% of states can be removed, which depended on the controller's complexity. This state-removing results in performance improvement both in XBM AFSM synthesis and technology independent hazard free logic minimization stages. The reshuffled controllers were usually synthesized to more compact circuit-level implementations.

Title: *Modified Odd-level Transistor Replacement*

Abstract:

The idea of a new static CMOS complex-gate mapping algorithm was based on modifying the odd-level Transistor Replacement (OTR) technique. I call it Modified OTR (MOTR). MOTR is very similar to the traditional cell-library binding, but it does not require any fixed standard gate library. In this project, I emphasize on evaluating the circuit areas and delay costs by the dynamic programming approach. My tool picked up the best cover set based on the cost metrics. This prototype implementation forks to the Berkeley SIS for decomposition and variables factoring. The simulations showed 10% to 15% performance gain and usually smaller transistor network.

Title: *A CMOS Self-Timed Micro-Module Library*

Abstract:

In this project, I redesigned a subset micro-module cells from the Asyn2 library (FPGA based asynchronous cell library developed in the University of Utah). I modeled the major 35 self-timed components in VHDL for Epoch CMOS ASIC compiler. I also designed the same component set in full-custom layouts. I used both libraries to design an asynchronous instruction fetching (IF) unit. Comparing the compiled ASIC design and the full-custom version, the area overhead is more than 30%. And, the full-custom IF's average cycle time was about 40% faster than the ASIC design. However, the design time and complexity also increased dramatically for the full-custom design.

RESEARCH INTERESTS

My research interest is in the area of low power high performance digital VLSI applications. This includes micro-architectures that reduce switching activity, dynamic logic families to operate at deep submicron and sub-1V supply voltage, algorithms for automated design and analysis procedures, and transistor-level optimization techniques for ultra-low voltage bulk and SOI CMOS. My immediate interest is in developing algorithms to better analyze state transition behaviors by employing Data-mining techniques over the simulated data. I hope to develop practical algorithms that address not only transition properties but also inductive effects caused by triggering input patterns. I would like to guide the algorithm development with a design project targeting a low power high performance application.

TEACHING INTERESTS

Having been impacted by many gifted teachers, I hope to likewise impact students at an undergraduate and graduate level. I hope to be able to contribute to a high standard of teaching excellence. I feel that my background has prepared me to teach a variety of courses including: computer architecture, logic design, VLSI design, low power VLSI design, computer-aided design of VLSI systems, asynchronous design, embedded systems, engineering electronics, VHDL, algorithms, computer programming, database, web-base applications and etc.

CAREER GOALS

My goal is build an open minded environment where ideas can be explored and developed freely. I hope to be able to provide students with the things they need to be successful in academic and research accomplishments. This is not just limited to technical knowledge. It includes friendship and genuine concern for their well being. It is my belief that when a student is successful, so is a professor and anyone else who has contributed along the way.

HONORS

- Nationwide Computer System Design Contest (Taiwan) - Awarded
- Intercollegiate Student VLSI Design Contest (USA) - Awarded
- University of Utah Engineering Dean's List

RESEARCH EXPERIENCE

- **Research Assistant for Associate Professor Erik Brunvand**
  May 1998 to present
  - ☑ Advanced computer architecture
  - ☑ Applied database and Web Services technologies for EDA designs
  - ☑ Asynchronous VLSI synthesis/design automation
  - ☑ Dynamic CMOS logic design and synthesis
  - ☑ Employed dynamic logic for self-timed datapath components
  - ☑ Low-power/high-performance VLSI Design
  - ☑ Technology mapping for extended Burst-Mode (XBM) controllers
  - ☑ Transistor-level optimization for XBM controller and datapath
  - ☑ XBM controller reshuffling
- **R&D Engineer for TAI-E Electrical Machining Co.**
  May 1990 to December 1990
  - ☑ Designed a real-time unit converter (Intel 8051)
  - ☑ Developed a firmware for a custom-build floppy driver (Motorola 6805)
- **Taiwan Nationwide Computer System Design Contest**
  May 1989 to January 1990
  - ☑ Centralized control center with dual-monitors (IBM PC)
  - ☑ Business applications
  - ☑ Developed a scalable security system
  - ☑ Developed distributed monitoring module (Motorola 68705)
  - ☑ Modified RS-232 protocol (master-slave bus system)
  - ☑ System firmware (Motorola 68705 and Intel 80286)

TEACHING EXPERIENCE

- **Teaching Assistant for Associate Professor Erik Brunvand**
  - Helped developing emulator for advanced computer architecture
  - Read and graded report and homework
  - Provided homework and emulator enhancement solutions
  - Managed grading information
- **Tutoring for Digital System Design and Programming Language**
  - Answered and explained homework problems
  - Helped students on programming assignments
- **Teaching programming language (Taiwan)**
  - Basic, C, Pascal for business application programming
  - 8088/86 system driver developing
- **Teaching assistant for Digital Circuit Design (Taiwan)**
  - Assisted lab practices
- **Tutoring for senior projects (Taiwan)**
  - Assisted database application developing
  - Assisted simple robotic control interpreter developing

PROFESSIONAL & DESIGN EXPERIENCE

- Assisted implementing asynchronous micro-engine by Xilinx FPGA
- Assisted in the design of an Asynchronous MPEG decoder employed Xilinx FPAG
- Built 16-Bit Min-RISC microcontroller by Actel FPGA
- Built a complete pipelined VHDL model of a CR-16 microprocessor
- Designed a Web board CGI script to help research discussion over the Internet
- Designed a real-time unit converter for numerical controllers
- Designed a set of scripts to simplify SPICE simulation and information extraction
- Designed a simple compiler supports subset of object-oriented features
- Designed an Entity-Relationship (ER) diagram generator
- Designed an extendable semi-bundled delay asynchronous adder
- Designed an intelligent security system for a small community
- Designed and verified a high speed asynchronous comparator
- Designed, fabricated, and test a natural logarithm component
- Re-design a subset components of the Async2 self-timed Cell Library

LANGUAGE

- Fluent in reading, writing, and speaking Mandarin
- Fluent in reading, writing, and speaking English
- Fluent in listening Cantonese

REFERENCES

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PUBLICATIONS

- Jung-Lin Yang, Erik Brunvand. "*Self-Timed Design with Dynamic Domino Circuits.*" In IEEE Computer Society Annual Symposium on VLSI, February 2003 (Accepted)

Abstract

We introduce a simple hierarchical design technique for building high-performance self-timed components using dynamic domino-style circuits. This technique is useful for building handshaking style functional blocks and for self-timed data path components. We wrap the dynamic domino circuit in a wrapper that communicates using a req/ack protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. The circuit overhead required for this early-acknowledge feature is relatively small, but can provide measurable speedup in some situations. We call this approach semi-bundled delay (SBD). SBD wrapped circuits allow a designer to take advantage of high-speed dynamic data path circuits that can be used with any self-timed or asynchronous design style that relies on an explicit completion acknowledge signal.

- Jung-Lin Yang, Erik Brunvand. *"Semi-Bundled Wrappers for Self-Timed Dynamic Domino Circuits."* In IEEE International Symposium on Asynchronous System & Circuits, May 2003

Abstract

We introduce a simple hierarchical design technique for using dynamic domino circuits to build high-performance self-timed data path circuits. We wrap the dynamic domino circuit in a wrapper that communicates using a re-quest/acknowledge protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. We call the resulting wrapper semi-bundled because of this early acknowledge. The circuit overhead required for this semi-bundled feature is relatively small, but can provide measurable speedup in some situations. The technique is suitable for any dynamic logic family that has a pre-charge/evaluate cycle, and that produces monotonic output transitions.