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Jung-Lin Yang

Objective A teaching/researching position in computer science/engineering, electrical engineering, or digital VLSI CAD tools development

Education **University of Utah** - Salt Lake City, UT **Degree: PhD and MS**
Major: Electrical & Computer Engineering **Date:** 2003-05-31

PhD Dissertation *Transistor-level Technology Mapping for Generalized C-element (gC) Implementation of XBM Controller*

In this research, I developed a transistor-level technology mapping technique for multiple input change (MIC) fundamental mode asynchronous controllers. The major contribution of this work is a pre-layout technology mapper and a design methodology to utilize it for asynchronous VLSI design. This technology mapper takes a set of synthesized raw generalized C-element (gC) equations and environment specifications in either burst-mode (BM) or extended BM (XBM) format. Transition probabilities are extracted from the given environment specification for optimization and hazard-preserving transformation purpose. The gC equations are then mapped into a transistor network for the target CMOS technology. All transistors in the mapped network are sized either by designers or my automatic sizing procedure based on optimization cost metrics. This technology mapper does not make any assumption for the gC implementation and controller specifications, any high-level BM/XBM synthesis tool can be used to generate technology independent raw gC equations needed. The pre-layout optimization strategies explored in this research can also be adopted to improve bundled-data delay self-timed datapath components.

Other Research *Self-Timed Design with Dynamic Circuits*

We introduce a simple hierarchical design technique for building high-performance self-timed components using dynamic domino-style circuits. This technique is useful for building handshaking style functional blocks and for self-timed data path components. We wrap the dynamic domino circuit in a wrapper that communicates using a req/ack protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. The circuit overhead required for this early-acknowledge feature is relatively small, but can provide measurable speedup in some situations. We call this approach semi-bundled delay (SBD). SBD wrapped circuits allow a designer to take advantage of high-speed dynamic data path circuits that can be used with any self-timed or asynchronous design style that relies on an explicit completion acknowledge signal.

Other Interests

- VLSI CAD Tools design and implementation
- Dynamic CMOS & SOI (silicon-on-insulator) logics design/synthesis
- FPGA/DSP/MCU circuits design/synthesis
- Advance computer architecture
- Object-oriented & Component-oriented programming
- Web/Database applications, E-Commerce, and Data mining for engineering

Honors

- Nationwide Computer System Design Contest (Taiwan) – Awarded
- Intercollegiate Student VLSI Design Contest (USA) – Awarded
- Dean's List (University of Utah)

Experience

1998-05-01 ~
Now

Graduate Student & Research/Teaching Assistant

University of Utah, Salt Lake City, UT

- ☑ Asynchronous VLSI circuits and systems design
- ☑ VLSI CAD tools development for asynchronous VLSI
- ☑ Extend-burst mode (XBM) controller reshuffling for performance improvement
- ☑ Technology Mapping for generalized C-element (gC) Implemented XBM Controller
- ☑ Teaching assistant for Advanced Computer Architecture
- ☑ CMOS transistor-level circuit synthesis CAD tools for self-timed datapath component

1996-09-01 ~
1998-04-30

Undergraduate Student

University of Utah, Salt Lake City, UT

- ☑ CMOS Implementation of Micro-module Asynchronous Cell Library
- ☑ Tutoring for Digital System Design and Object-oriented Programming Language
- ☑ 16-Bit Min-RISC Microcontroller: PowerView schematics and synthesizable VHDL
- ☑ VLSI circuit design contest for US university/college students - awarded

1990-05-01 ~
1990-12-31

CNC Controller Hardware & Software Developer

TAI-E Electron Machining Co., Taiwan ROC

- ☑ Developing computer base (embedded system) numerical controller to enhance the traditional NC machine
- ☑ Motorola 68010 CPU and Intel 8051 microcontroller systems design (C and Assembly)

1988-05-01 ~
1989-06-30

Business Application Programmer & Programming Instructor

Chin-Haw Computer, Kaoshoung, Taiwan ROC

- ☑ Developing financial and accounting applications in Pascal, C, and dBase III
- ☑ Teaching Basic, C, Pascal for business application programming
- ☑ Teaching assembly language for system driver developing

1985-06-01 ~
1990-05-31

College Student

South Taiwan University of Technology, Taiwan, ROC

- ☑ Intelligence Security System for a Small Community – awarded by the Taiwan nationwide Computer System Design Contest
- ☑ Teaching assistant for Digital Circuit Design
- ☑ Tutoring for senior projects (Database Application and Simple Robotic Control)

Computer Skills

Languages:

C, C++, C#, Java, Visual Basic, Object-Pascal (Delphi), Python, Perl, Scheme, Fortran, SQL, VHDL, Verilog, and some Assembly languages (Z80, Intel 8088/8086/8051, Motorola 68010/68705/68HC11, MIPS 4000, PIC)

Operating Systems:

UNIX (Linux, SunOS), MS Windows

Applications:

MS Visual Studio (6.0 and .Net), MS Office XP, MS Visual Modeler, MS VISIO, MS SQL Server, Matlab, Maple V, Cadence PSpice, HSpice, Cadence (IC Design), PowerView, Active-HDL, Oracle Database Server 8i/9i, MySQL, Spy XML, Berkeley SIS, and some Unix/Linux based tools

Reference

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