

Self-Timed Design with Dynamic Domino Circuits

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Abstract

We introduce a simple hierarchical design technique for building high-performance self-timed components using dynamic domino-style circuits. This technique is useful for building handshaking style functional blocks and for self-timed data path components. We wrap the dynamic domino circuit in a wrapper that communicates using a request/acknowledge protocol and mediates the pre-charge/evaluate cycle of the dynamic logic. We apply standard bundled delay matching for completion detection but add an early completion feature that can signal completion if function validity can be determined from the output value. The circuit overhead required for this early-acknowledge feature is relatively small, but can provide measurable speedup in some situations. We call this approach semi-bundled delay (SBD).