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### **Abstract**

The research presented in this proposal concerns a transistor-level technology mapping technique for extended-burst-mode (XBM) asynchronous controllers. XBM is a flexible class of multiple-input change (MIC) fundamental-mode state machines based on the burst-mode model. This kind of machine is quite similar to a traditional synchronous finite state machine (FSM) in many ways but not controlled by clock edges. Thus, experienced synchronous digital system designers can apply them in their future designs easily. Moreover, this class of controllers is an excellent bridge between existing synchronous systems and asynchronous systems. Thus, it provides a possible solution to the clock and block communication network skew problems in system-on-chip (SOC) designs. Our goal in this research is to build a pre-layout technology mapper and to provide a design methodology for asynchronous VLSI system design. We are going to design a technology mapping technique that performs technology-dependent transistor mapper for arbitrary generalized C-element (gC) networks synthesized from XBM specifications. This tool will also handle transistor sizing and signal ordering based on pre-defined cost metrics such as delay and/or power consumption. Circuit layout area consideration might be added when we learn more about automatic leaf-cell layout generators. The pre-layout optimization strategies explored for the controllers can also be adapted for bundled-data delay datapath components as well. This is made possible by applying UC Berkeley logic synthesis tool SIS with our task completion detection wrapper. The end result will be a design flow to utilize our tool for asynchronous system design.