Ali Ibrahim

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Research Interests

- Low-Power and Energy-Aware System design
- Computer Architecture
- Reconfigurable Computing
- VLSI design
- Wireless Communication

Education

- **University of Utah**—SLC, UT
  Ph.D. in Electrical and Computer Engineering May-26 2005
  Advisor: Prof. Al Davis
  Dissertation: A high Performance Energy-Aware Adaptive Cellular Telephony (ACT) coprocessor.
- **University of Rome La Sapienza**—Rome, Italy
  Laurea in Electronic Engineering July 1999
  Advisor: Prof. M. G. Benedetto.
  Dissertation: FPGA Based Digital Signal Processing-Study of An Adaptive Echo canceler.

Research Experience

- **AMD Inc, Discrete Graphic Division**— January/7/2007-Present
  Power estimate from Spreadsheet to netlist.
  Power optimization: System level, Architecture, Micro-architecture, RTL, Netlist.
  Power management
  Leading the development of PowerRed which is "An architecture level power modeling infrastructure for GPUs.
- **Co-founder of Satva design automation**— June/2/2005-Dec/31/2006
  A high tech start-up company with Siemens as angel investor.
- **Research Assistant, School of Computing**—Prof. Al Davis Summer 2003-May/18/2005
  ACT Processor I proposed a high performance, low-power, yet flexible coprocessor for wireless applications.
- **Research Assistant, School of Computing**—Prof. Al Davis Spring (Jan) 2003-Summer 2003
  The perception Processor I worked on the design and implementation of a high performance, low-power perception processor.

- **Research Assistant, School of Computing**—Prof. John Carter Fall 2000-Fall (Dec) 2002
  Micro Architecture and VLSI for an Adaptive High Performance Memory Controller I showed that the performance of SDRAM-based memory system can be improved by Memory Controllers that intelligently schedule multiple requests and take advantage of bank parallelism available within the SDRAM chips. Furthermore, the improvement can be achieved with a small increase in chip area
- **Intern, Ericsson Telecommunication, Rome,Italy**—Eng. C. Porfiri Fall 1998-Summer 1999
  FPGA-based digital signal processing-Study of an adaptive echo canceler. The scope of the work was the evaluation of Programmable Logic in comparison with digital signal processors when the algorithms require high computing power per device.

Ph.D. Research: ACT

Future mobile terminals need to support higher data rates, full motion video and multimedia applications, a variety of wireless standards, be energy efficient, flexible, and have a low time to market and be low in cost. The computational requirements imposed by these applications and standards have increased exponentially (faster than Moore's law) since the introduction of the first generation wireless telephony (1G).

The traditional approach for applications requiring both performance and low-power is to employ ASICs for compute intensive components. In areas where applications evolve rapidly, flexibility is also an important factor and a general purpose or embedded processor approach has often been used for this reason. For applications such as wireless communications, voice, and video processing: ASICs are too inflexible and costly; low-power processors do not have sufficient computational power; and general purpose processors consume too much power. This situation motivates this investigation of an alternative approach.

The key in designing for low power, high performance, and flexibility relies on finding opportunities for customization for a particular domain. There could be a high number of parameters involved in this process (memory system, single- vs. multi-cluster, bypass logic, register files, compression, and function unit design). Each of these parameters can have a big effect on the performance, power, and flexibility.

In ACT, a high energy-delay product efficiency was achieved through software controlled distributed memories, modulo addressed distributed single ported register files, multi-level reconfigurable interconnects, semi-reconfigurable address generation units, SIMD-ALUs, compression techniques, context switching, and extra hardware to support special wireless operations. The processor is basically a fine-grain VLIW architecture. The fine-grained software control provides considerable generality, and efficiency in terms of energy-delay product since different pipelines can be dynamically reconfigured to support a new processing phase that resembles data flows found in an ASIC implementation.

For a range of algorithms taken from 3G wireless, DSP and MPEG kernels, the processor is within one to two orders of magnitude of the energy-delay product of an ASIC and three to four orders of magnitude more efficient than a low power embedded processor implementation. Energy and performance numbers for ACT were calculated using Synopsys Nanosim, a commercial Spice level circuit simulator, on a fully synthesized and back-annotated .25μm Verilog- and Module Compiler-based implementation.

Publications(In Press or Under Review)

- A. Ibrahim, M. Parker, and A. Davis. Energy efficient cluster coprocessors. International

Conference on Acoustics, Speech, and Signal Processing, May 2004.

- B. K. Mathew, A. Davis, and A. Ibrahim. Perception coprocessors for embedded systems. Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), 2003.
- A. Ibrahim and A. Davis. Address acceleration mechanisms for an adaptive cellular telephony processor. International Conference on Multimedia and Expo (ICME05), 2005.
- A. Ibrahim and A. Davis. Exploiting data context switching in a low power VLIW coprocessor. Workshop on Optimizations for DSP and Embedded Systems (ODES), in conjunction with IEEE/ACM International Symposium on Code Generation and Optimization (CGO), 2005.
- A. Ibrahim, A. Davis, and M. Parker. ACT: A low power VLIW cluster coprocessor for DSP applications. Workshop on Optimizations for DSP and Embedded Systems (ODES), in conjunction with IEEE/ACM International Symposium on Code Generation and Optimization (CGO), 2006.
- Zhen Fang, Lixin Zhang, John Carter, Ali Ibrahim and Mike Parker. Active memory operations. International conference in supercomputing (ICS), 2007
- PowerRed: A Flexible Power Modeling Framework for Power Efficiency Exploration in GPUs. Karthik Ramani, Ali Ibrahim and Dan Shimizu. Worskshop on General Purpose Processing on Graphics Processing Units (GPGPU), 2007
- J. Mahovsky, B. Wyvill, A. Davis, A. Ibrahim. Robust Ray-Bounding Volume Hierarchy Traversal with Reduced Precision Integer Arithmetic. Submitted to Journal of Graphics Tools, 2005.
- ACT: Adaptice Cellular Telephony Coprocessor. Ali Ibrahim. PhD thesis. 2005
- FPGA Based Digital Signal Processing-Study of An Adaptive Echo canceler. Ali Ibrahim. Laurea (Master equivalent) thesis. 1999

Book Chapter

- Stream processors and their application to the wireless domain. Binu Mathew,Ali Ibrahim. Digital Systems and Applications, CRC Press LLC, 2007.

Basic Skills

- VLSI design with Verilog, VHDL
- Programming languages: C, C++, Python, MIPS assembly language
- Tools: Synopsis Module Compiler, Design Analyzer, VCS, Nanosim, Silicon Ensemble, PrimeTimePX, PowerTheater, HSPICE, dc_shell scripting
- Architecture, micro-acrhitecture, C and verilog implementation of Mips, Stream, VLIW, and application specific processors. SOC design based on AMBA bus.

Graduate Courses

-Advance Computer Architecture -CAD of Digital Circuits -Embedded Systems
-Parallel Computer Architecture -Analog Circuits Design I -Analog Circuits Design II
-VLSI Architecture -Advance DSP I
Seminars:

-High Performance Memory Systems -Networking -Asynchronous Circuits

Courses at Haas Business School, University of California Berkeley

-New Venture Finance
-Wireless Communication: Analysis of the industry structure, the value chain, the business models, the role of regulation and opportunities for start-ups and new entrants

Students

Supervised a PhD candidate from the school of computing, University of Utah, during his summer internship at AMD, May/2007 to September/2007

Other Activities

Reviewer for IEEE International Conference on Sensor and Ad hoc Communications and Networks
Reviewer for International Journal in Computer Networks(COMNET).
Reviewer for ACM Multimedia
Reviewer for ACM/SPIE Multimedia Computing and Networking (MMCN)
Reviewer for the Journal of Systems and Software (elsevier)

References

- Per request....