

Hemanthkumar Sivaraj

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OBJECTIVE

To obtain a full-time position in Formal Verification or Software Systems

EDUCATION

- Dec 03 **M.S. Computer Science**
University of Utah, Salt Lake City, UT
GPA: 3.98/4.00
- May 99 **B.E. (Hons.) Computer Science**
Birla Institute of Technology and Science (BITS), Pilani, India
Major GPA: 9.76/10.00
Overall GPA: 8.76/10.00
- May 99 **M.Sc. (Hons.) Mathematics**
Birla Institute of Technology and Science (BITS), Pilani, India
Major GPA: 9.42/10.00
Overall GPA: 8.76/10.00

AREAS OF INTEREST

Application of Formal Verification Techniques to System Design, Construction of CAD tools, Computer Networks, Distributed Systems, Voice over IP (VoIP)

WORK EXPERIENCE

Jun. 99 – Jun. 00 Software Engineer Hughes Software Systems, Bangalore, India

- Worked with the ITU-T H.323 protocol as part of the Gatekeeper product team in the Voice over IP (VoIP) group. Involved in the product development from the design specification to the implementation and testing stage. The implementation was done in C.
- Designed and developed a Session Initiation Protocol (SIP) to H.323 Gateway that was demonstrated at a Voice on the Net (VON) interoperability event.
- Was part of a study group formed to study about the WAP protocol stack and to propose an architecture for a WAP Gateway.
- Was part of a team that won a **Team Award** for performance.

TECHNICAL SKILLS

Programming Languages	C/C++, Java, Perl, Ocaml, Pascal, x86/MIPS/SPARC assembly, lex, yacc
Operating Systems	Linux, Sun Solaris, FreeBSD, Windows (NT, 9x)
Verification Related	Murphi, SPIN, Promela, Cache coherence protocols, formal/semi-formal verification, SAT (Boolean Satisfiability) tools
Other Technologies	TCP/IP, UDP, MPI programming, Voice over IP (VoIP) protocols, H.323, SIP
Programming Experience	Object Oriented Analysis and Design, Network Programming, Client Server Programming, Strong Linux and Unix experience/background

RESEARCH EXPERIENCE

Jan 04 – Present: Research Assistant, Utah Verifier Group

Project: *Verification of shared memory data consistency in MP code sequences*

Currently implementing a memory ordering tool that will verify if a given shared memory MP code sequence is allowed by the Intel Itanium memory ordering model. This is to be used as part of post-silicon processor verification. The tool is being implemented in Ocaml. Other tools that are used are lex and yacc.

Jan 02 – Dec 03: Research Assistant, Utah Verifier Group

Masters Thesis Title: *Random Walk Based Heuristic Enumerative Distributed Memory Model Checking*

Advisor: Ganesh Gopalakrishnan (<http://www.cs.utah.edu/~ganesh>)

Designed, implemented, and evaluated heuristics that combine parallel random walks with exhaustive state space search techniques like breadth-first search to increase the bug hunting efficacy of an explicit state model checker. The software was developed using C, C++, and MPI programming for distributed communication.

Aug 01 – Dec 01: Research Assistant, Utah Verifier Group

Project: *MPI implementation of Parallel Murphi*

Ported the parallel version of the model checker Murphi to use MPI as the message passing layer.

May 01 – August 01: Research Assistant, Utah Verifier Group

Worked towards enabling the in-house model checker PV to be used as a backend for the Bandera toolset that extracts finite state models from Java source code

Jan. 99 – Jun. 99: Intern, Chennai Mathematical Institute

Worked with Dr. Madhavan Mukund (madhavan@smi.ernet.in) and Dr. Narayan Kumar (kumar@smi.ernet.in) on the formal specification) and verification of the communication protocol ITU-T recommendation Q.704. PROMELA and SPIN were used for specification and verification.

Aug. 98 – Dec. 98: Bachelor Thesis, Birla Institute of Technology and Science, Pilani, India

Advisor: Prof. J.P. Misra (jpm@bits-pilani.ac.in)

Evaluated the performance of a Two-Level Rollback Recovery Scheme for Fault Tolerance in Distributed Systems.

PUBLICATIONS

- G. Gopalakrishnan, Y. Yang, H. Sivaraj, *QB or not QB: An Efficient Execution Verification Tool for Memory Orderings*, In 16th International Conference on Computer Aided Verification (CAV'04), Boston, Massachusetts, July 2004.
- H. Sivaraj, G. Gopalakrishnan, *Parallel Random Walk Based Heuristics for Semi-Formal Verification*, TECHCON 2003, Dallas, USA, August 2003.
- H. Sivaraj, G. Gopalakrishnan, *Random Walk Based Heuristic Algorithms for Distributed Memory Model Checking*, 2nd International Workshop on Parallel and Distributed Model Checking (PDMC'03), Boulder, Colorado, USA, July 2003.
- P. Chatterjee, H. Sivaraj, G. Gopalakrishnan, *Shared memory consistency protocol verification against weak memory models: refinement via model-checking*, In 14th International Conference on Computer Aided Verification (CAV'02), Lecture Notes in Computer Science, Copenhagen, July 2002. Springer-Verlag.

TEACHING EXPERIENCE

Jan. 01 – May. 01: **Advanced Algorithms and Data Structures**, University of Utah

Aug. 00 – Dec. 00: **Computer Architecture**, University of Utah

RELEVANT COURSES

Foundations of Computer Science, Advanced Computer Architecture, Compilers, Programming Languages and Semantics, Data Communications and Networking, Advanced Networking, Computer Systems Seminar, Data Structures, Digital Electronics and Computer Organization

COURSE PROJECTS

- Implementation and Performance Evaluation of On-Demand Multicast Routing Protocol (ODMRP) for Ad-Hoc Networks in the ns-2 network simulator.
- Overlay Network for Digital Content Delivery.
- Web server and a text based web client
- Compiler for a Java like OO language
- Design and Implementation of a User Level Threads Library in UNIX
- Implementation of the Tomasulo and Scoreboarding algorithm inside a simulator for the DLX processor
- Implementation of a Client Server Application to simulate a multi-user OS
- Implementation of a Multi-user chat application.

REFERENCES

Prof. Ganesh Gopalakrishnan
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Additional references are available upon request.