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### **PROFESSIONAL OBJECTIVE**

A position where my research skills and experience with algorithm development and circuit design techniques in the area of VLSI design can be utilized to the long term benefit of research and development within an industry leading organization.

### **QUALIFICATION HIGHLIGHTS**

- Strongly self-motivated, reliable, and resourceful. Equally effective working independently or collaboratively in a team effort.
- Research experience in developing architectures and control techniques for high performance VLSI designs. Detailed understanding of heterogenous clocking techniques and circuit design techniques for power sensitive environments.
- Experienced in algorithm and tool development for synthesis of VLSI system designs.

### **EDUCATION**

Ph.D., Computer Science, emphasis on VLSI design, currently ongoing education.  
University of Utah, Salt Lake City, UT

Master of Science, Computer Engineering, emphasis on VLSI design, 1996.  
Lulea University, Lulea, Sweden.

Recipient of the 1999 University of Utah Graduate Research Fellowship award.  
University of Lulea Karhuset 1992 ITS work-team manager.

### **EXPERIENCE**

- Co-op. IBM T.J. Watson Research Center, Yorktown, N.Y., Jan 2001 - present.
  - Devised a new concept allowing progressive stalling and stage interlocking of traditional synchronous pipelines. Developed new correct-by-construction techniques for automated clock gating at the register macro level.
- Internship. IBM T.J. Watson Research Center, Yorktown, N.Y., Summer 2000.
  - Researched and developed low-power techniques and circuit structures for issue logic in high-performance microprocessors.
- Research Assistant. University of Utah, Department of Computer Science, 1995 - 2001.
  - Developed a design framework for high-level synthesis of high performance asynchronous system designs.
  - Developed a high performance general architecture for asynchronous programmable circuits for domain-specific applications.
  - Developed low latency partitioned control structures for finite state machine based system design.
  - Developed a unified approach for fast and exact logic minimization of speed-independent and extended burst-mode asynchronous controllers.
- Research/Teaching Assistant. Lulea University, Sweden, 1994-1995.
  - Developed parts of a rapid prototyping system of synchronous digital systems using high capacity FPGA's and PCB's.
  - Implemented low-level support libraries for the Modula-3 object oriented programming language.

## RESEARCH INTERESTS

- Micro-architectures, circuit structures, and heterogenous clocking techniques for high-speed, low-power microprocessors.
- Simultaneous multi-threaded architectures for high instruction throughput and resource utilization in synchronous and asynchronous microprocessor systems.
- High-level design and synthesis of asynchronous system level designs, including high-speed architectures for hardwired and programmable control.
- Fast and exact algorithms for unified synthesis, logic minimization, and technology mapping of asynchronous and synchronous finite state machines.

## PUBLICATIONS

- "Efficient Algorithms for Exact Two-Level Hazard-Free Logic Minimization." *Hans Jacobson and Chris Myers. In proceedings of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol.21, No.11, Nov 2002.*
- "Synchronous Interlocked Pipelines." *Hans Jacobson, Prabhakar Kudva, Pradip Bose, Peter Cook, Stanley Schuster, Eric Mercer, Chris Myers. In proceedings of the Eighth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC), April 2002.*
- "Efficient Exact Hazard-Free Two-Level Logic Minimization." *Chris Myers and Hans Jacobson. In proceedings of the Seventh International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC), March 2001.*
- "Power-Aware Microarchitecture: Design and Modeling Challenges for Next-Generation Microprocessors." *David Brooks, Pradip Bose, Stanley Schuster, Hans Jacobson, Prabhakar Kudva, Alper Buyuktosunoglu, John-David Wellman, Victor Zyuban, Manish Gupta, Peter Cook. In proceedings of the IEEE Micro, Vol.6, Nov/Dec 2000.*
- "Achieving Fast and Exact Hazard-Free Logic Minimization of Extended Burst-Mode gC Finite State Machines." *Hans Jacobson, Chris Myers, Ganesh Gopalakrishnan. In proceedings of International Conference on Computer Aided Design (ICCAD), 2000.*
- "High-Level Asynchronous System Design using the ACK Framework." *Hans Jacobson, Erik Brunvand, Ganesh Gopalakrishnan, and Prabhakar Kudva. In proceedings of Sixth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC), 2000.*
- "Application-Specific Programmable Control for High-Performance Asynchronous Circuits." *Hans Jacobson, Ganesh Gopalakrishnan. Proceedings of IEEE, Vol.87, No.2, February 1999.*
- "Asynchronous Microengines for Efficient High-level Control." *Hans Jacobson, Ganesh Gopalakrishnan. 17th Conference on Advanced Research in VLSI (ARVLSI), 1997.*
- "Synthesis of Hazard-free Customized CMOS Complex-Gate Networks Under Multiple-Input Changes." *Prabhakar Kudva, Ganesh Gopalakrishnan, Hans Jacobson, Steven Nowick. 33rd Design Automation Conference (DAC), 1996.*
- "A Technique for Synthesizing Distributed Burst-mode Circuits." *Prabhakar Kudva, Ganesh Gopalakrishnan, Hans Jacobson. 33rd Design Automation Conference (DAC), 1996.*
- "Imposing a Unified Design Methodology for Independent Rapid Prototyping Tools." *Anders Hedberg, Hans Jacobson, Mats Einarsson, Glenn Jennings. IEEE International Workshop on Rapid System Prototyping Hardware-Software Codesign, 1995.*
- "Design and Validation of a Simultaneous Multi-Threaded DLX Processor." *Hans Jacobson. Technical Report, UUCS-99-013, 1999.*