

OBJECTIVE

To pursue a full time position in the field of computer systems and software development

EDUCATION

Master of Science, in Computer Science, December 2008 (expected)

[School of Computing](#), University of Utah, Salt Lake City (Current GPA: 3.85/4)

Master's Thesis: "Perceptron-based Cache Coherence Predictors for CMPs" *Advisor*: [Dr. John Carter](#)

Bachelor of Technology, in Electrical and Electronics Engineering, May 2004

[National Institute of Technology, Tiruchirappalli](#), India (C.G.P.A. 9.3/10)

Department Rank 2 out of 64 students

PROFESSIONAL EMPLOYMENT

- Software Engineer at [ST Microelectronics](#), India for **2 years** (July 2004 to July 2006)
- Research /Teaching Assistant at School of Computing, University of Utah (Aug 2006 - Present)

RESEARCH WORK SUMMARY

Using machine learning to improve memory performance for shared memory multiprocessors:
Investigation, design and evaluation of hardware predictors that exploit data sharing patterns in multi-threaded applications, for accelerating cache coherence protocol operations.

REFEREED PUBLICATIONS

- **D. Ghosh, J. Carter, H. Daume III.** "[Perceptron-based Coherence Predictors](#)". In *Proc. of 2nd Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI), in conjunction with ISCA 2008.*

INDUSTRY WORK SUMMARY (STMicroelectronics, India)

- Functional verification of ST's multimedia System-on-Chip: Test-bench construction (C/Verilog), generation of test patterns (Specman/C), and verification of RTL simulation results against (SystemC) reference model
- RTL verification (NCSim) and post silicon testing of ARM9 based ADSL Router/Gateway.
- Device driver and other embedded software development (μ CLinux) and debugging for ADSL router.
- STMicroelectronics internal training in Embedded Systems, ARM Basics, Verilog HDL and NC Simulator.

HONORS AND AWARDS

- Dean's fellowship for 2nd rank in EEE department for junior and senior year at N.I.T. Trichy, India.
- DTSE (District Talent Search Examination) Scholarship, for the academic year 1996-1997, for overall scholastic abilities in the district of Uttar Pradesh, India.
- School topper and nationwide highest marks in physics in Grade 12, I.S.C. board examination.
- Ranked among the top 2% nationwide, in IIT-Joint Entrance Exam, year 2000.

PROJECTS (IN ACADEMIA)

- Sensitivity analysis to determine the impact of coherence message delays on performance of multiprocessors.
- Developed an operating system kernel (booting, process management, context switching, memory management, inter-process communication and other system calls) based on *Yalnix* emulation system.
- Developed *MiniJava* compiler (scanner, parser, IR-tree & Assembly code generator) for MIPS target, in Java
- Designed and implemented an online bookstore using MySQL and XML.
- Developed closed loop control of a single phase inverter on TMS320C2407 DSP. (B.Tech project).
- Verilog design and FPGA implementation of RGB/YCrCb color space converters (DRDO labs, Dehradun).

SKILLS

- **Programming Languages:** C, C++, Java, MATLAB, SQL/XML, Perl, Shell Scripts, Verilog HDL, JavaCC.
- **Parallel Programming:** Shared Memory (Pthreads), Message Passing (MPI).
- **Tools:** Cadence NCSim, ClearCase/RCS, ARM debugging tools (RVD, AXD), LaTeX.
- **Architecture Simulator:** Virutech Simics, Wisconsin GEMS, SimpleScalar.
- **Operating Systems:** Linux/Unix, Windows, Solaris, μ CLinux.

RELEVANT COURSES

Advanced Computer Architecture, Operating Systems, Compiler Principles and Techniques, Algorithms, Machine Learning, Database Systems, Scientific Computing, Computer Networks, Programming Languages (C/C++)

REFERENCES

Available upon request