MAIN MEMORY SYSTEM

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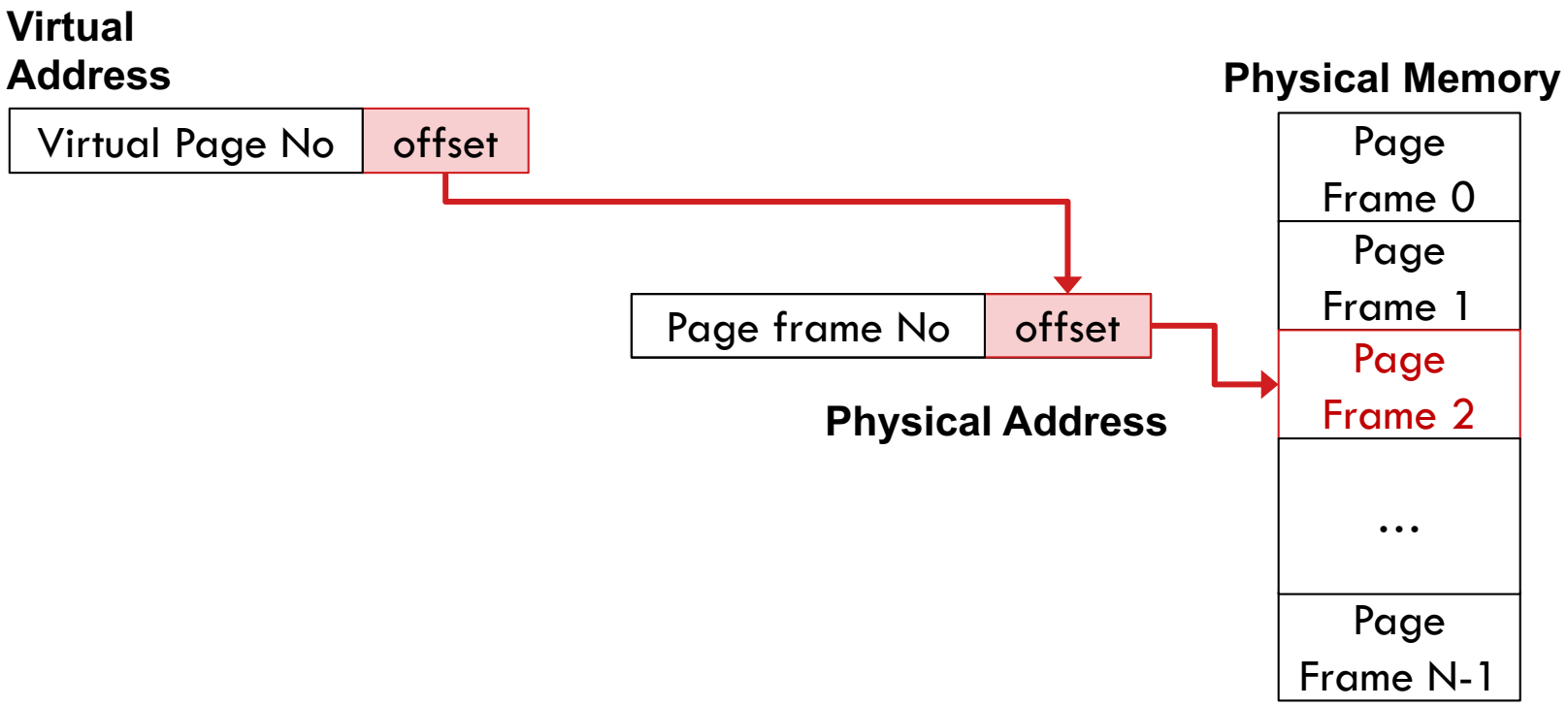
Overview

- Announcement
  - Homework 4 submission deadline: Nov. 6th
- This and the following lectures
  - Dynamic random access memory (DRAM)
  - DRAM operations
  - Memory scheduling basics
  - Emerging memory technologies

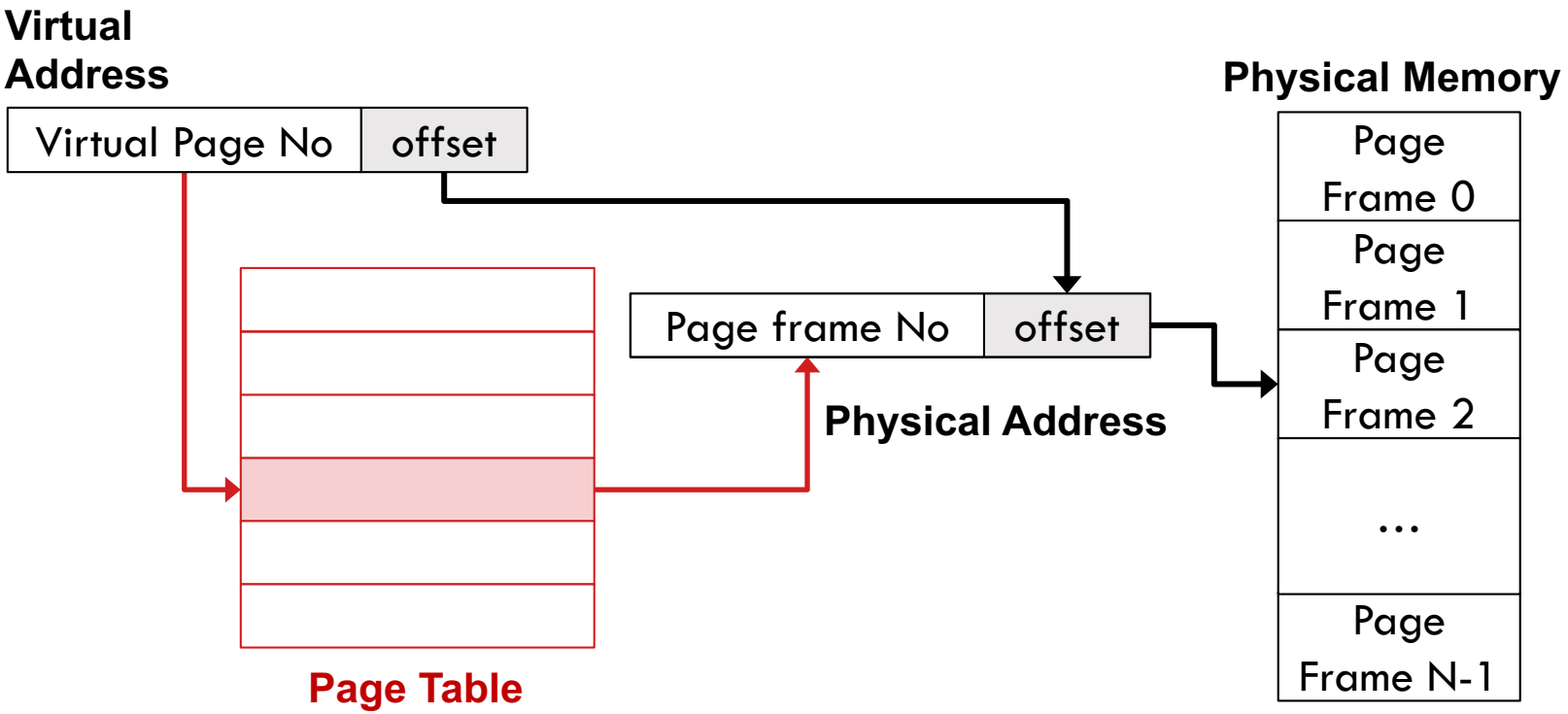
Recall: Address Translation

- Exploit locality to reduce address translation time
  - Offset bits are copied from virtual address



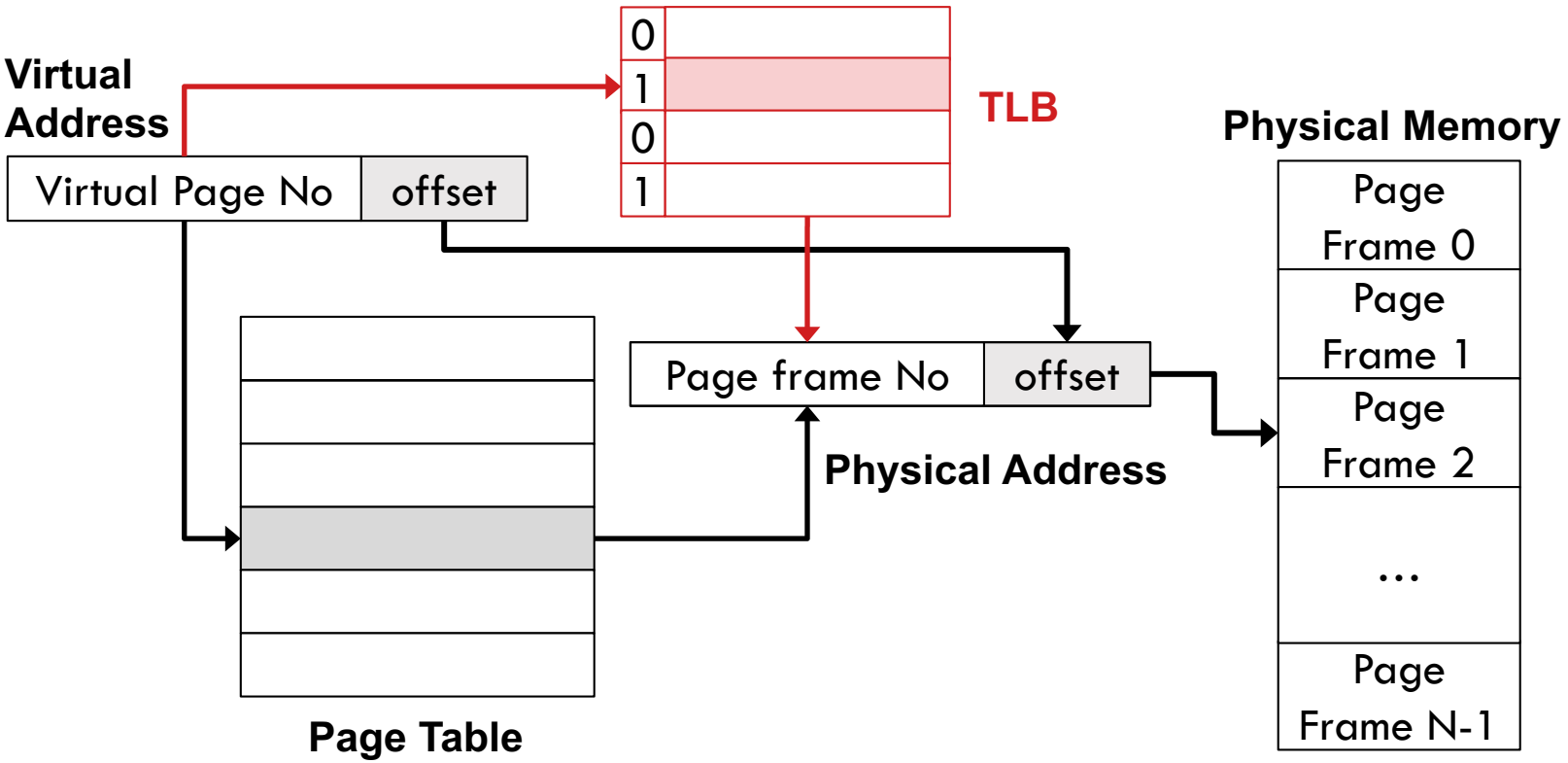
Recall: Address Translation

- Exploit locality to reduce address translation time
  - OS maintains the page table for address translation



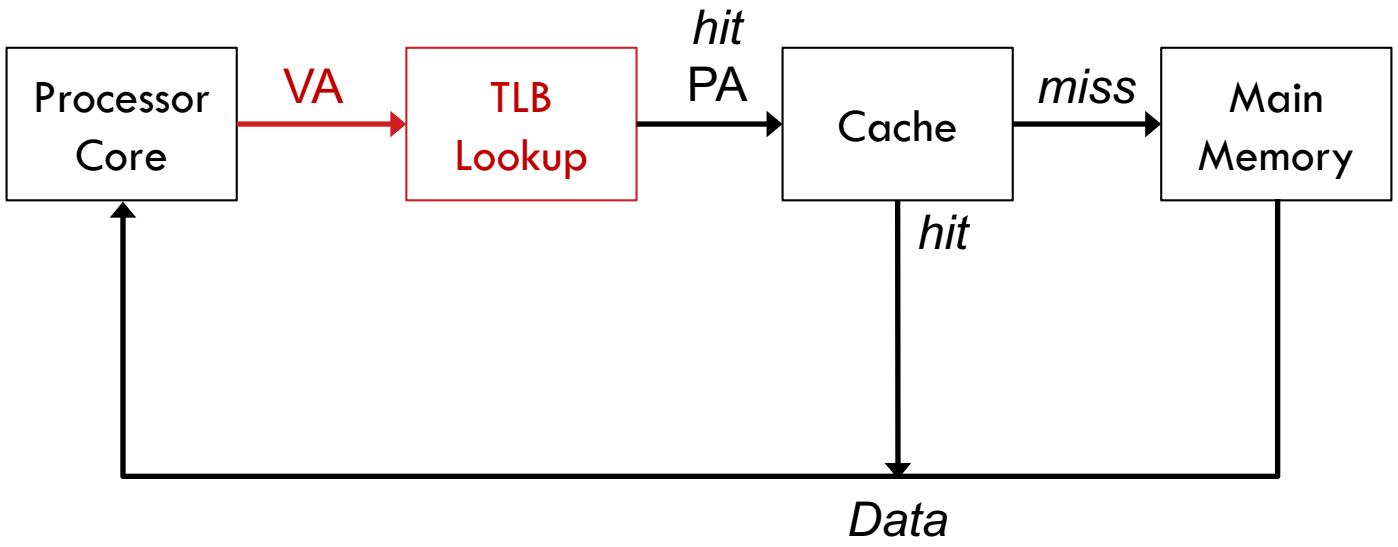
Recall: Translation Lookaside Buffer

- Exploit locality to reduce address translation time
  - Keep recent translation in a buffer for future references



TLB in Memory Hierarchy

- On a TLB miss, is the page loaded in memory?
  - Yes: takes 10's cycles to update the TLB
  - No: page fault
    - Takes 1,000,000's cycles to load the page and update TLB



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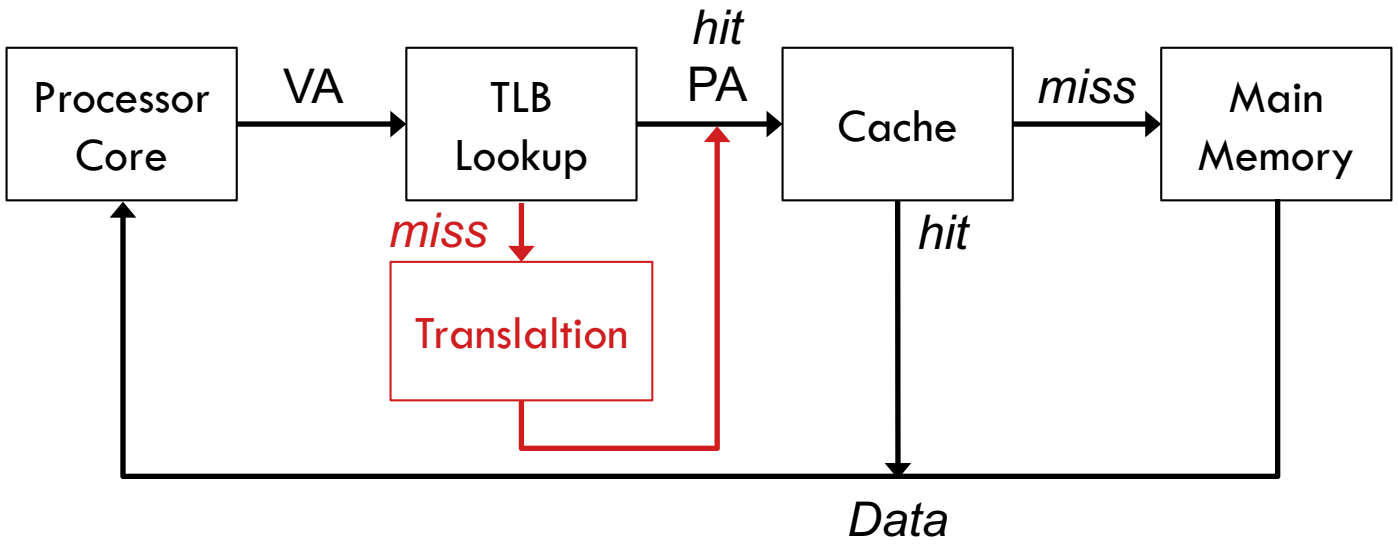

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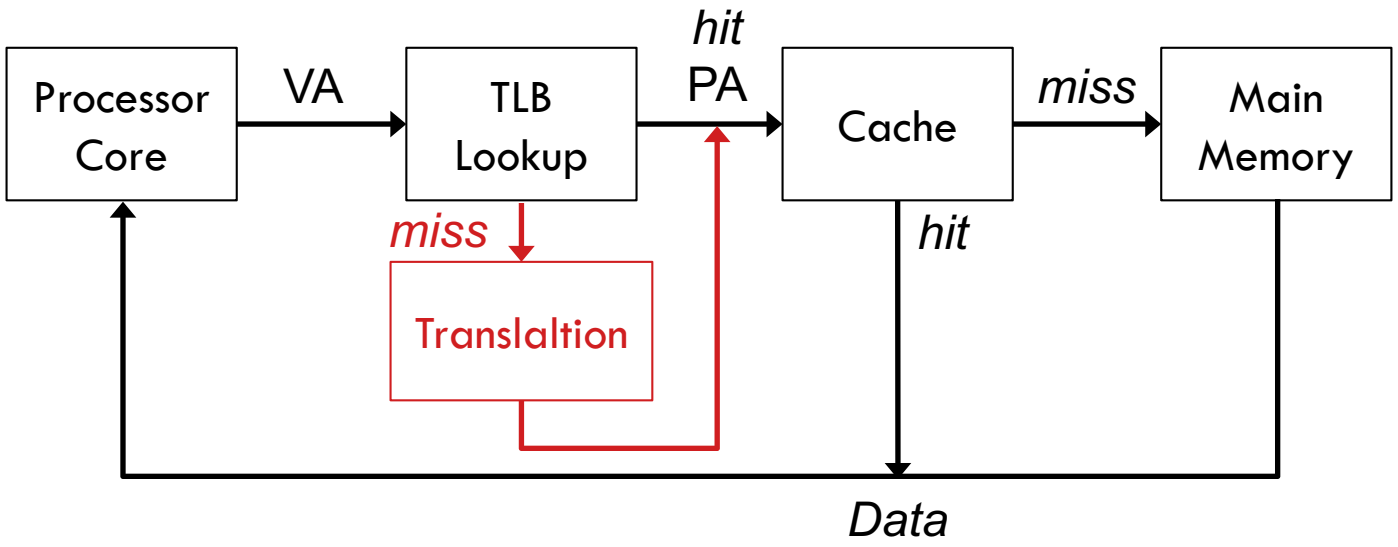
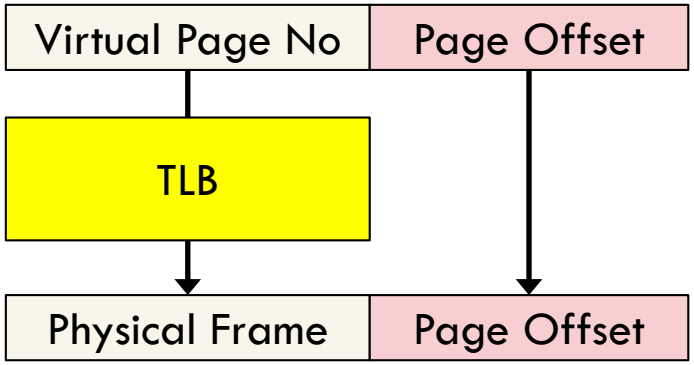
Physically indexed, physically tagged: TLB on critical path!



Physically Indexed Caches

- Problem: increased critical path due to sequential access to TLB and cache



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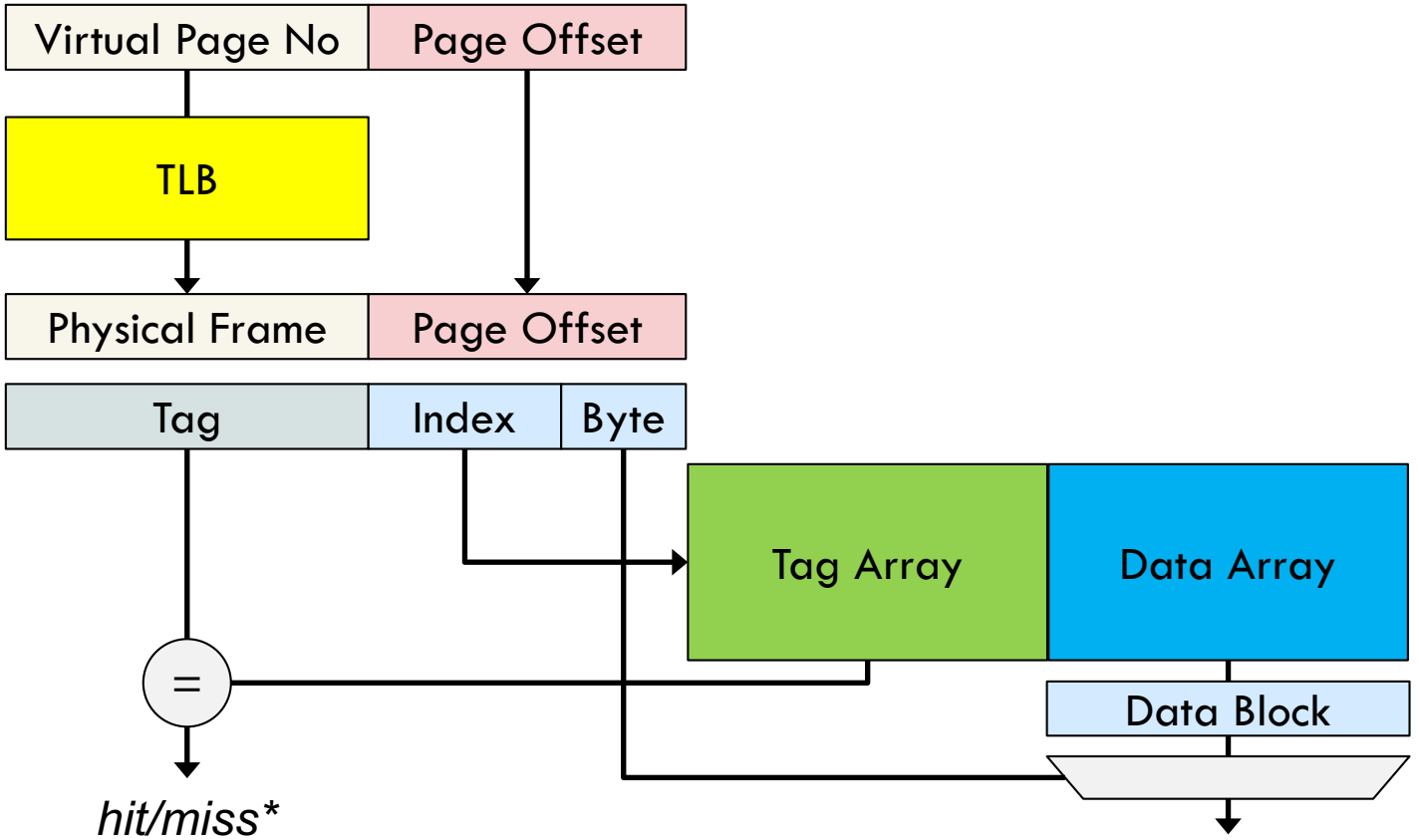

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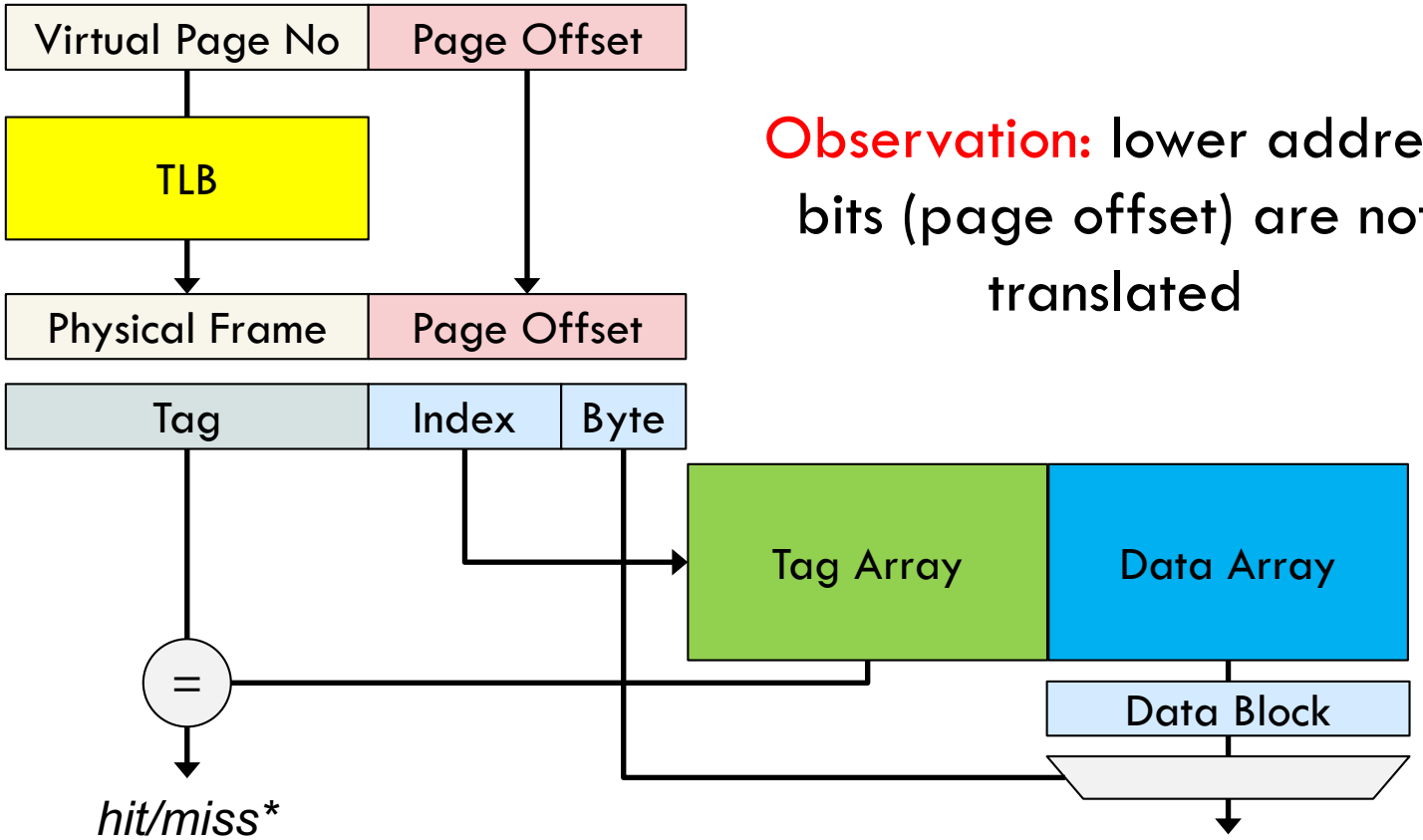
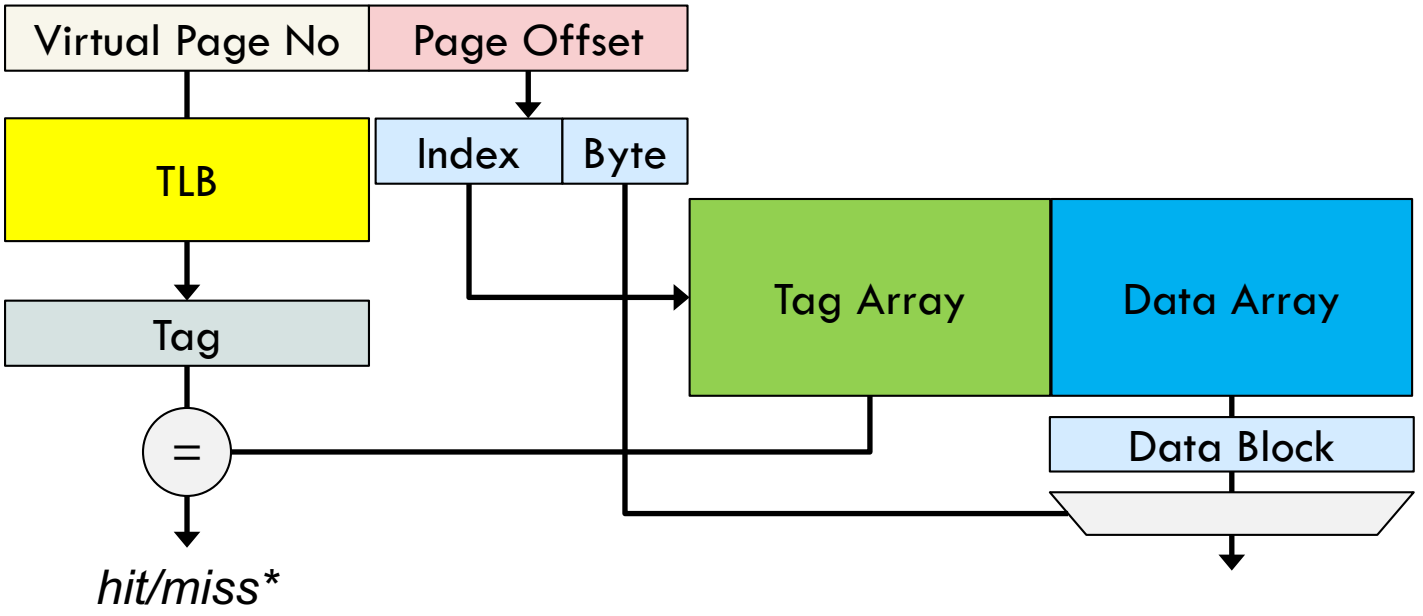


Observation: lower address bits (page offset) are not translated

Virtually Indexed Caches

- Idea: Index into cache in parallel with page number translation in TLB



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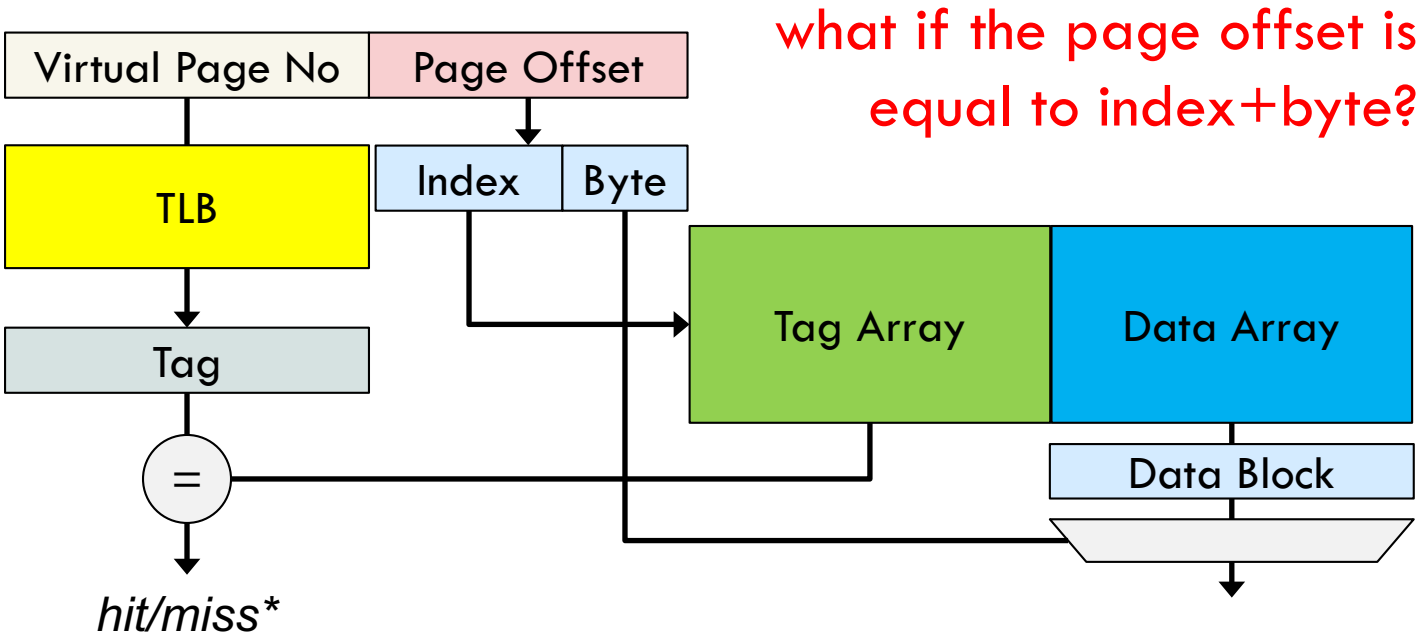

Main Memory

Computer System Overview

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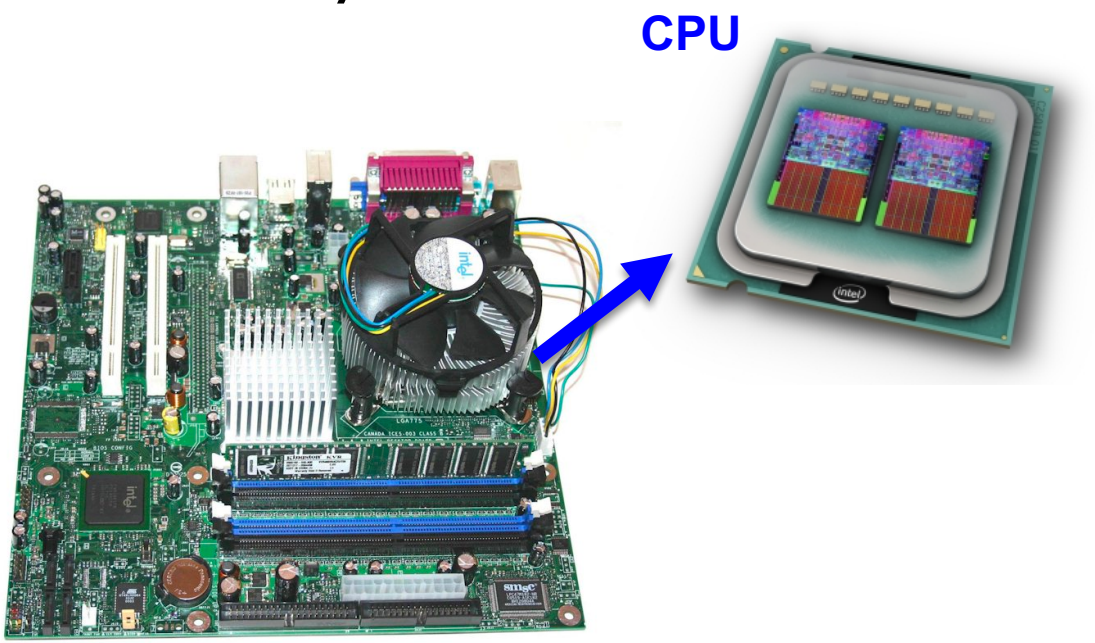

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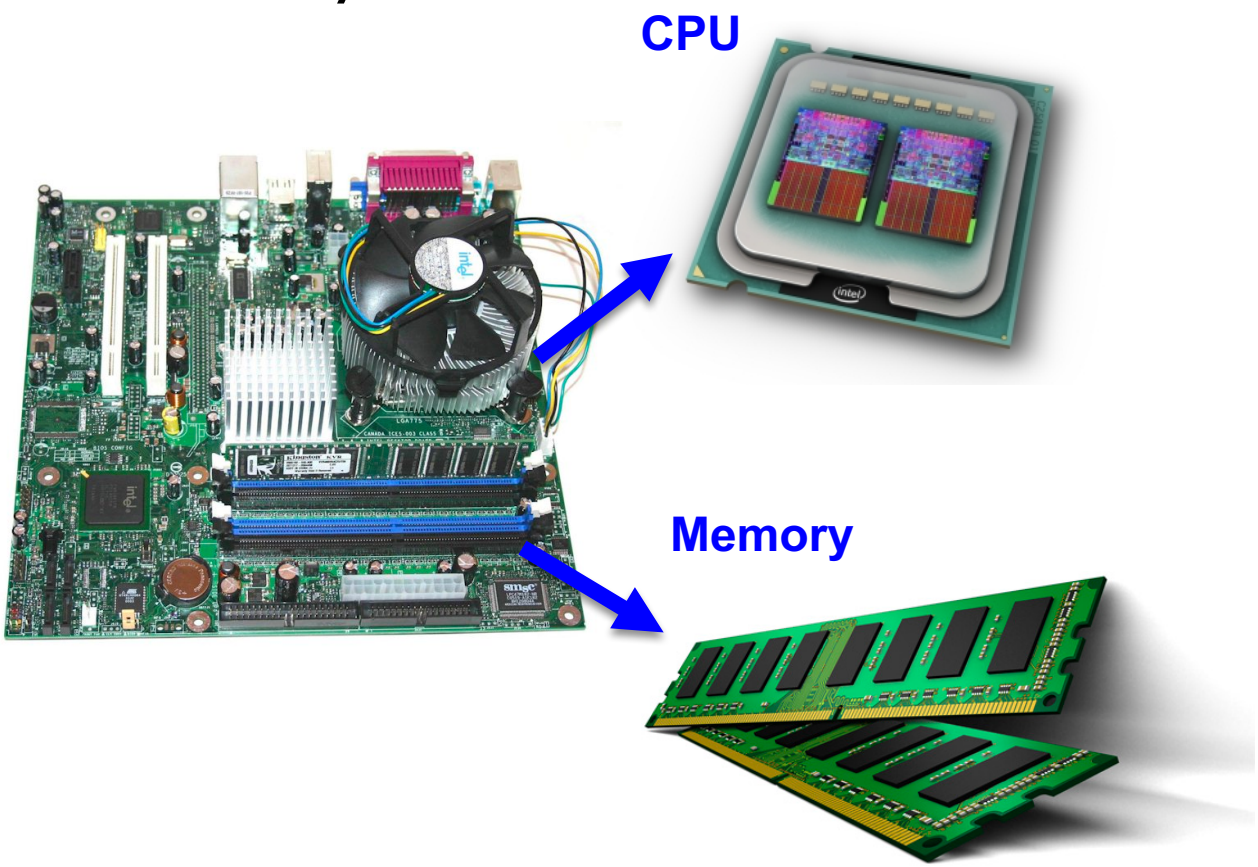

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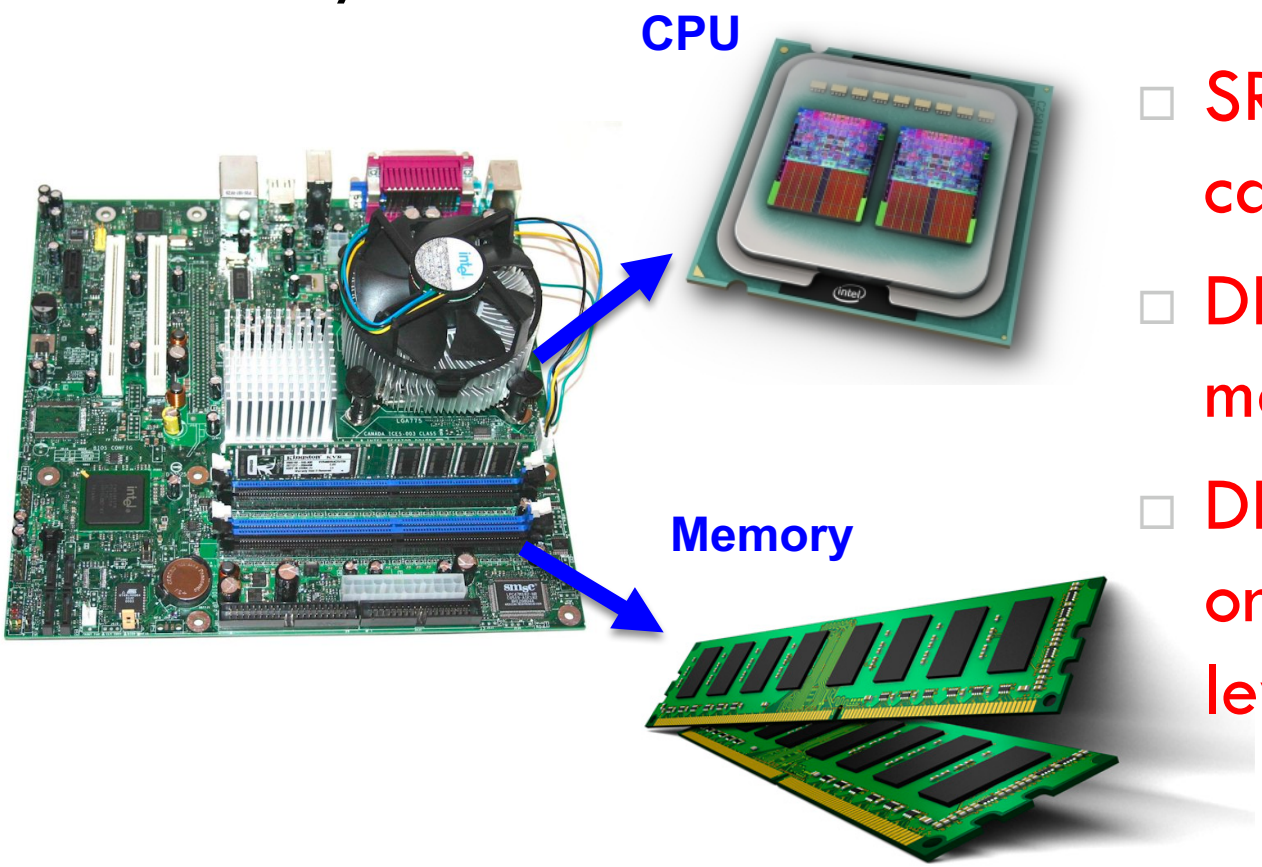
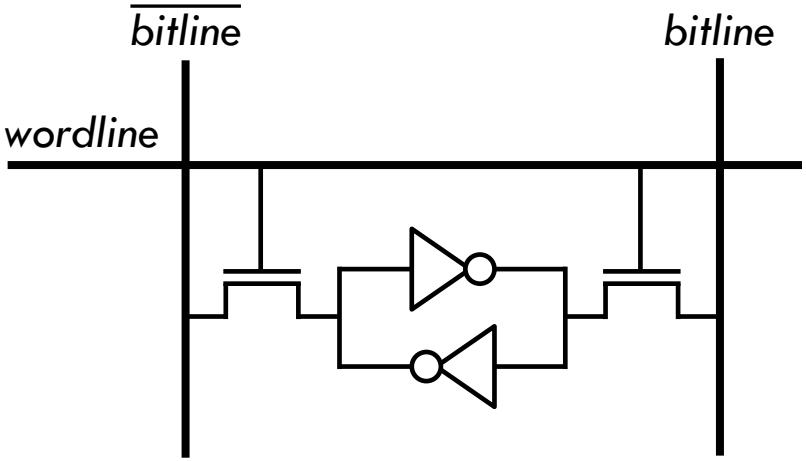


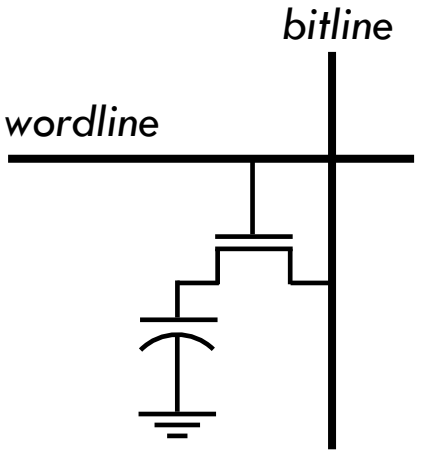
- SRAM is used for caches
- DRAM is used for main memory
- DRAM is accessed on a TLB or last level cache miss

Static vs. Dynamic RAM

Static RAM (SRAM)

Dynamic RAM (DRAM)





Static vs. Dynamic RAM

Static RAM (SRAM)

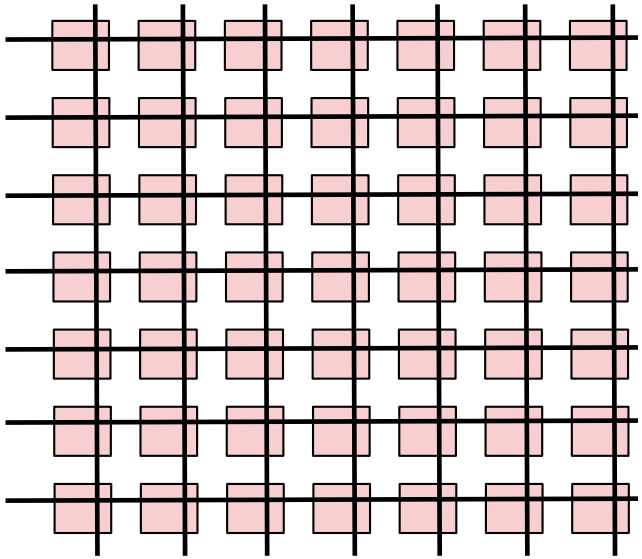
- Fast and leaky
  - 6 transistors per bit
  - Normal CMOS Tech.
- Static volatile
  - Retain data as long as powered on

Dynamic RAM (DRAM)

- Dense and slow
  - 1 transistor per bit
  - Special DRAM process
- Dynamic volatile
  - Periodic refreshing is required to retain data

DRAM Organization

- DRAM array is organized as *rows* × *columns*



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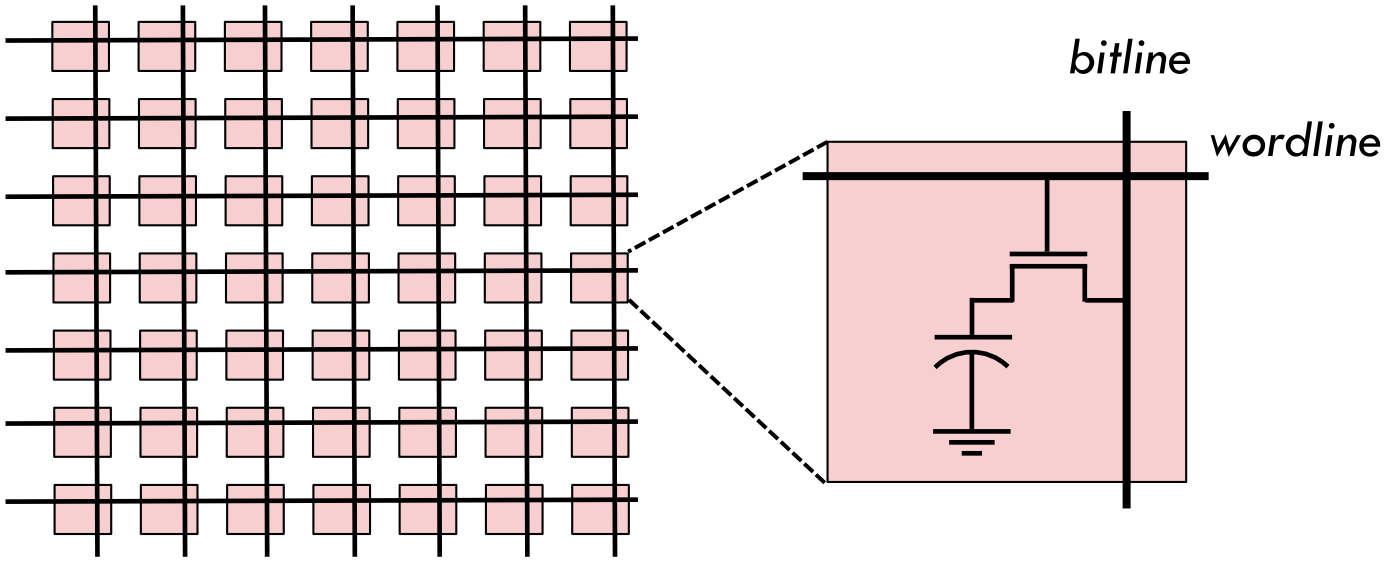

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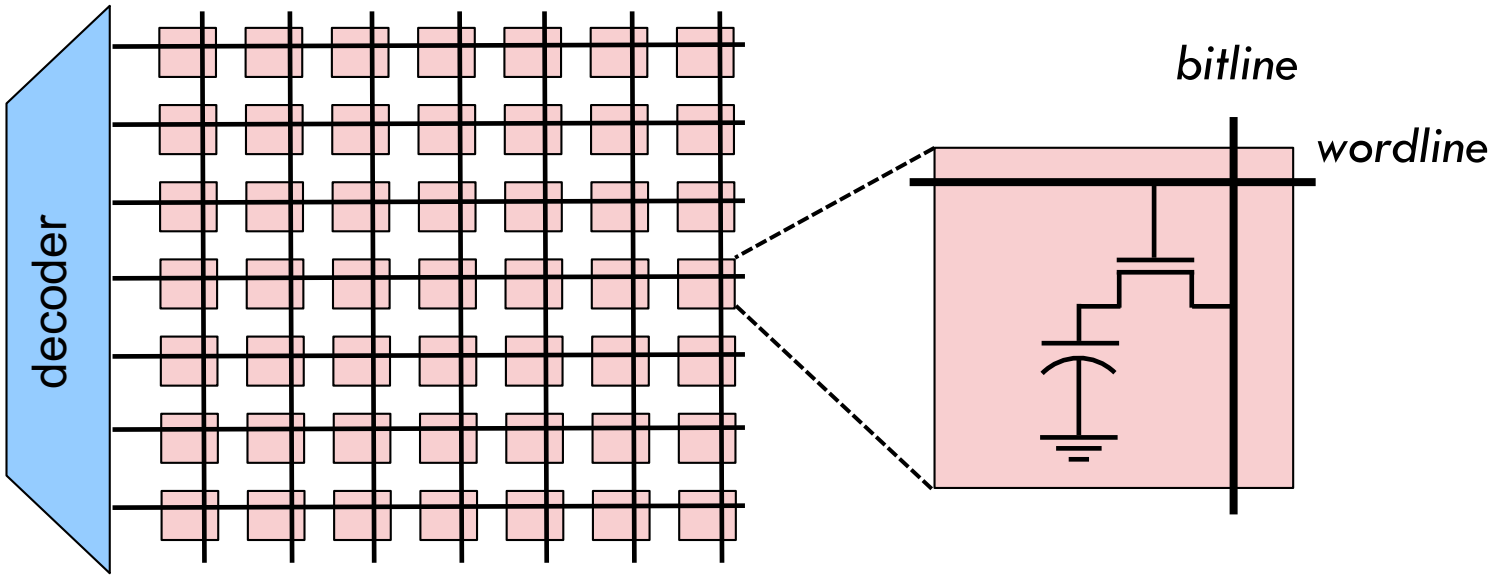

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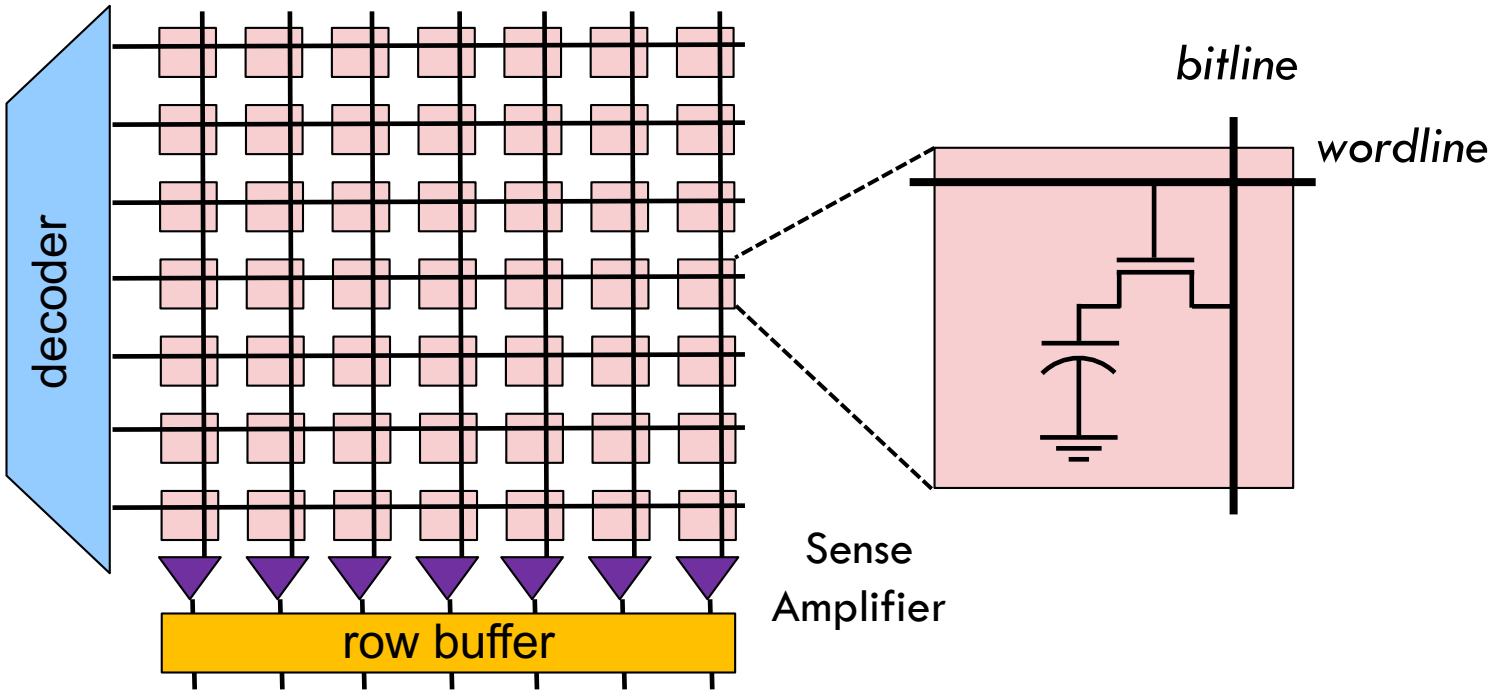

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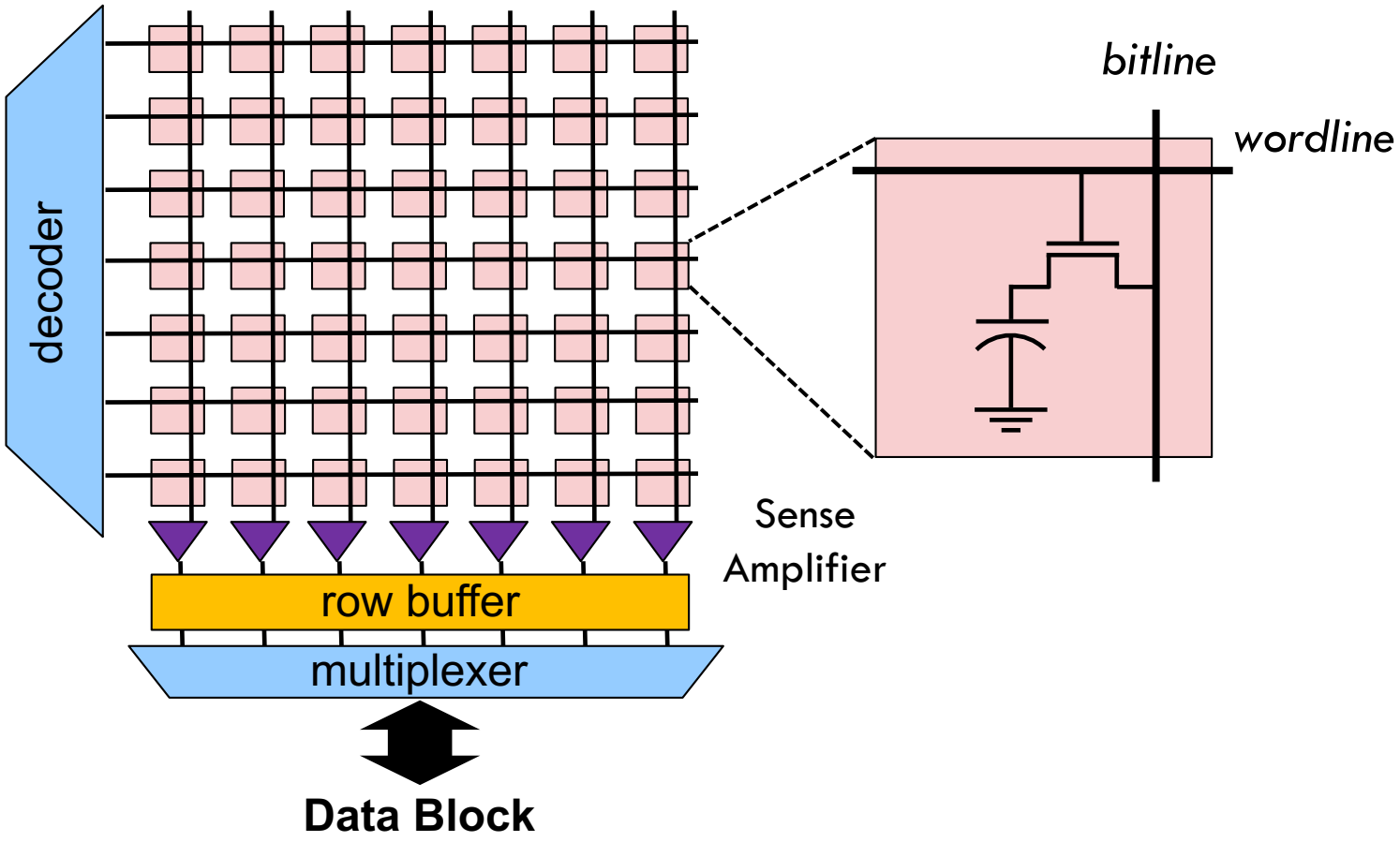

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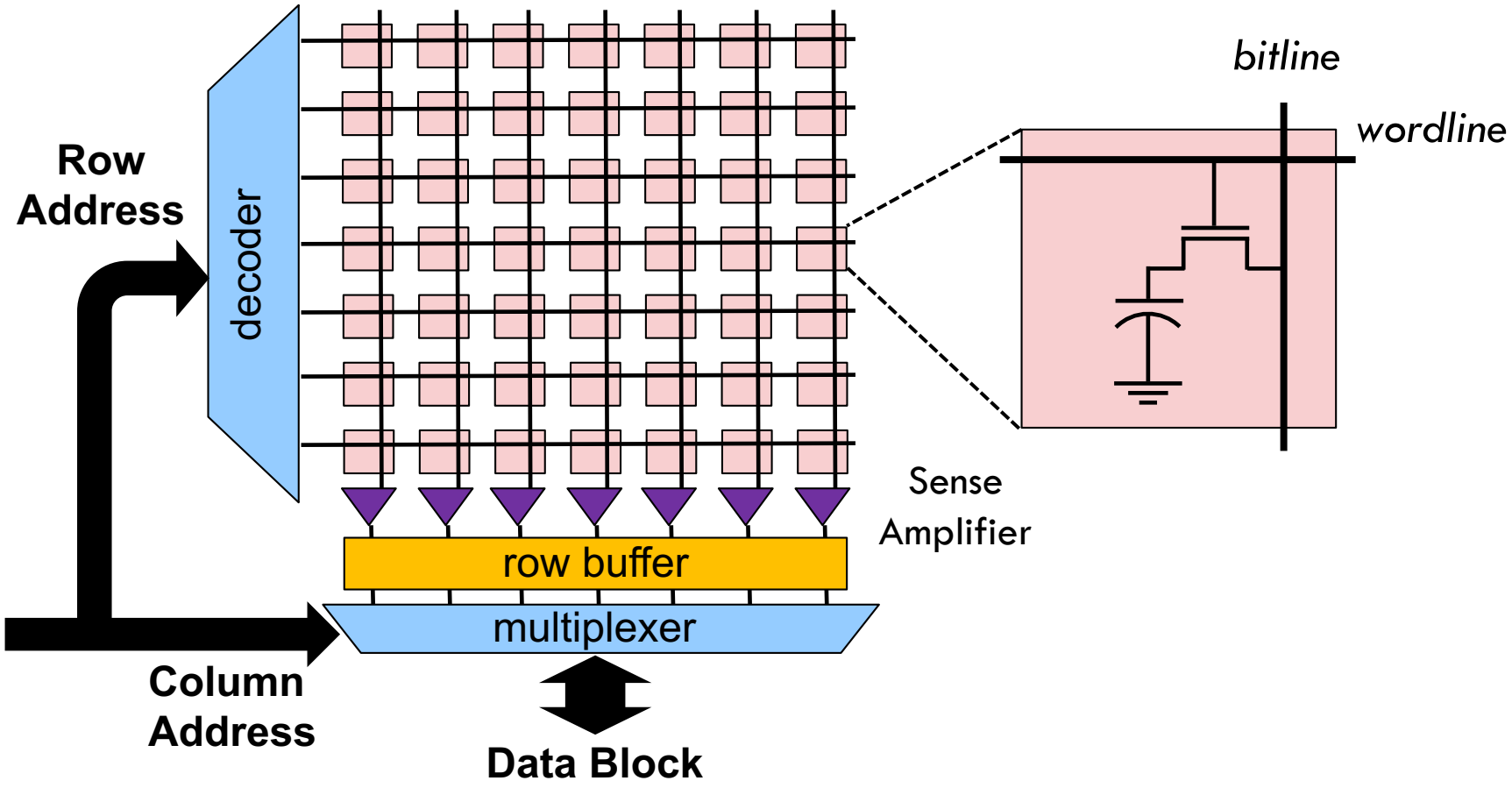

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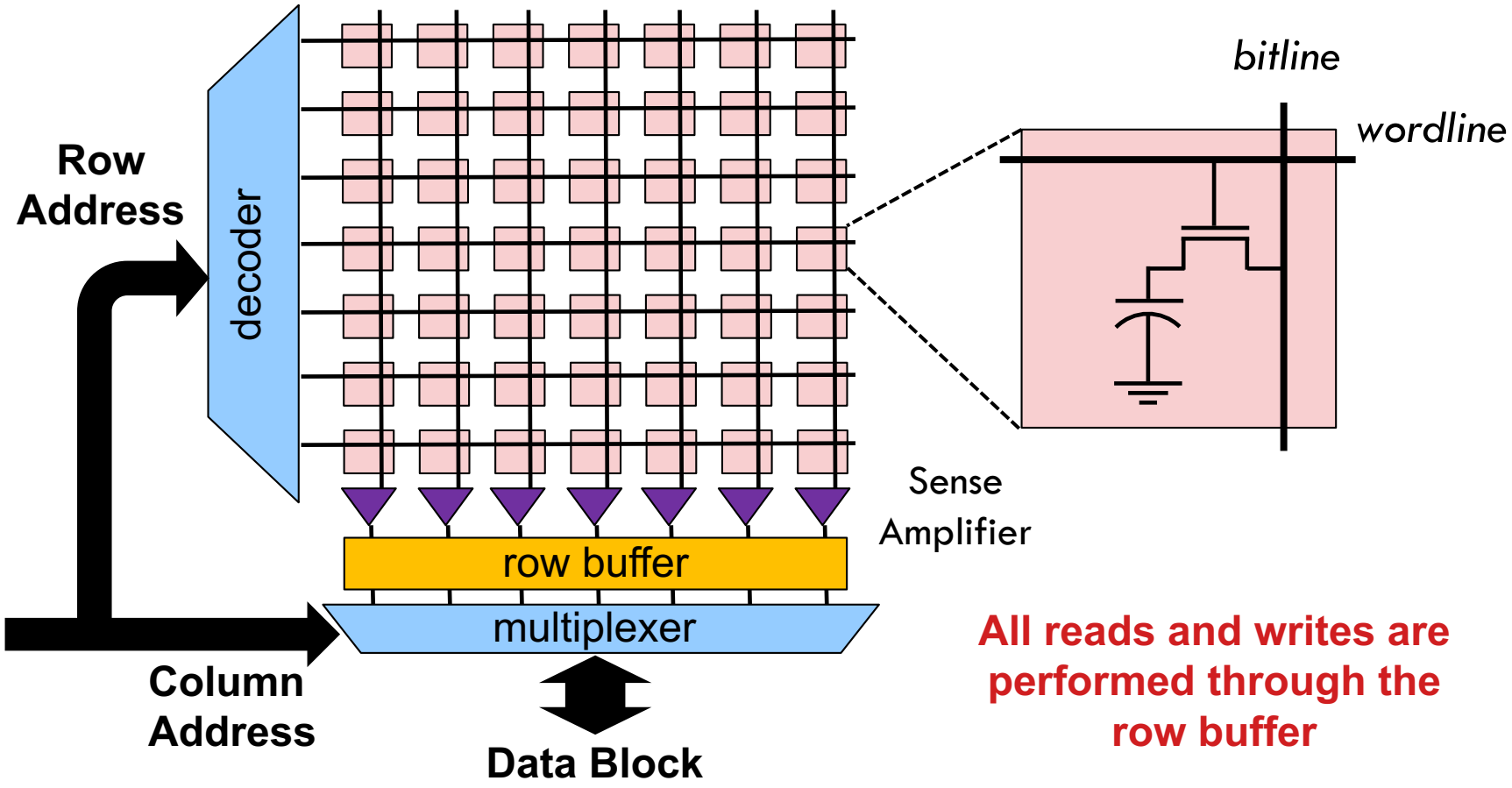
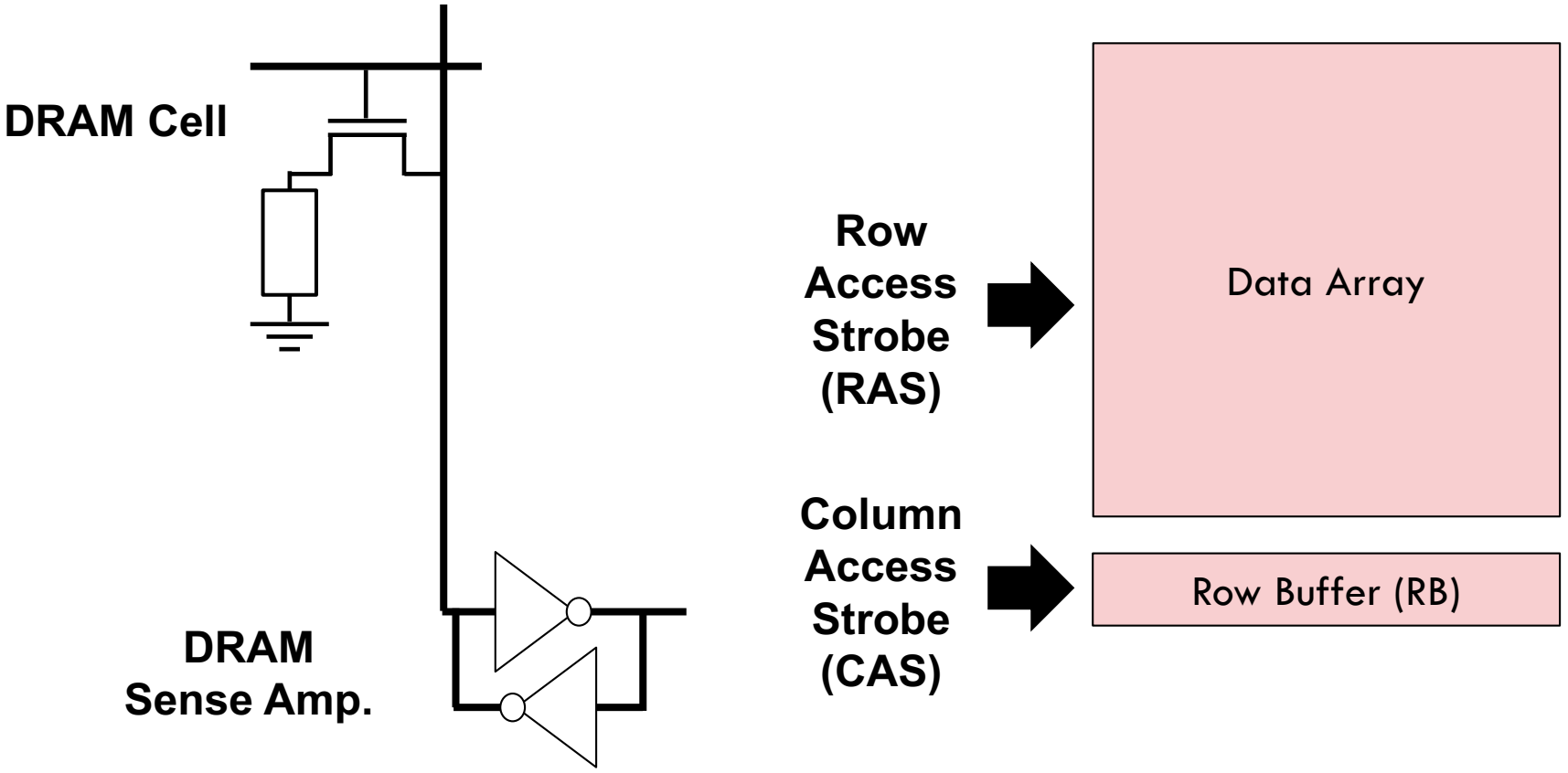


DRAM Row Buffer

- All reads and writes are performed through RB



Reading DRAM Cell

- DRAM read is destructive
  - After a read, contents of cells are destroyed

	Precharge	Activate	Sense
Reading a zero			
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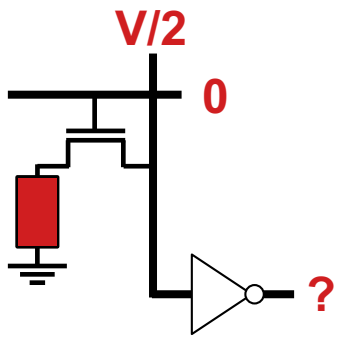
Reading a zero			
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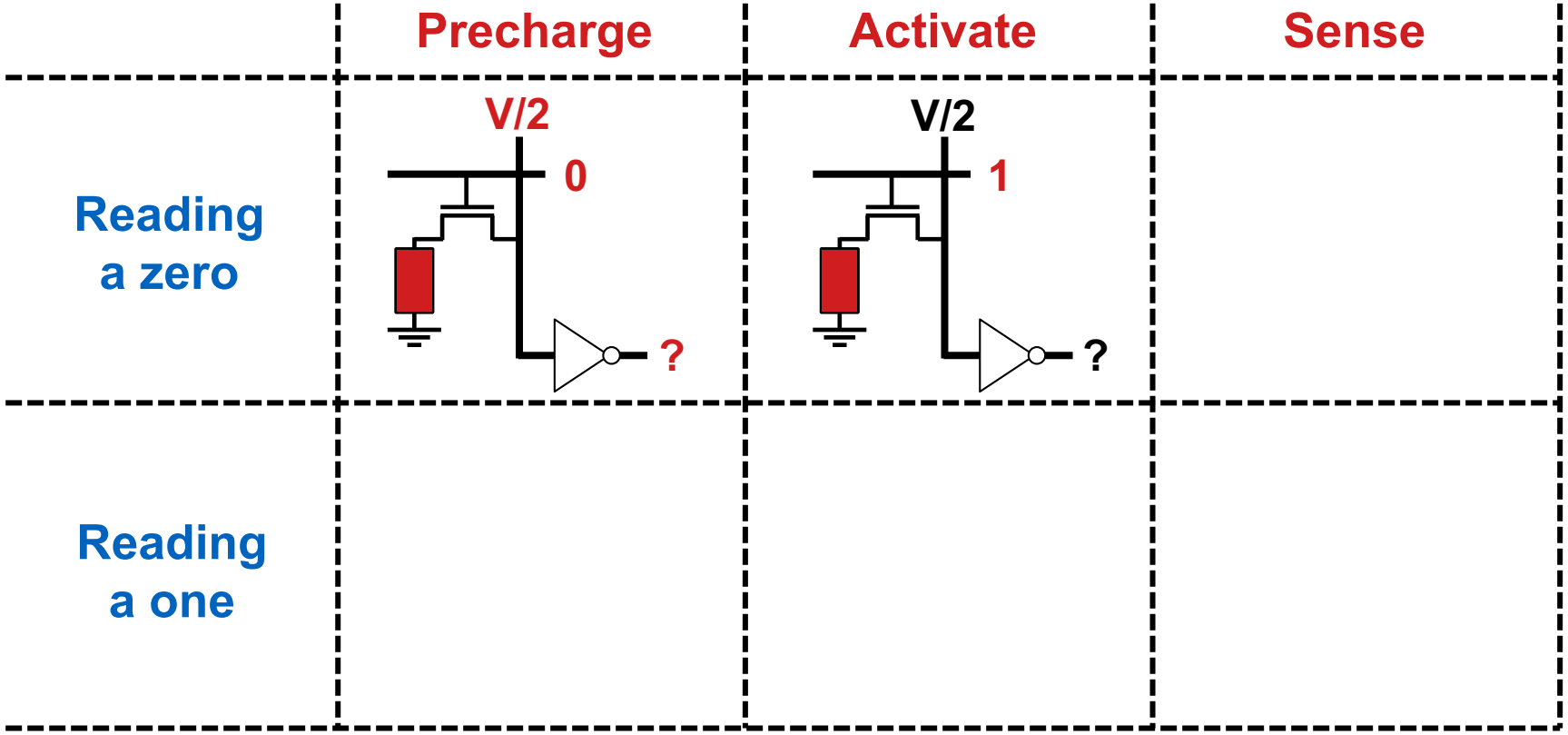

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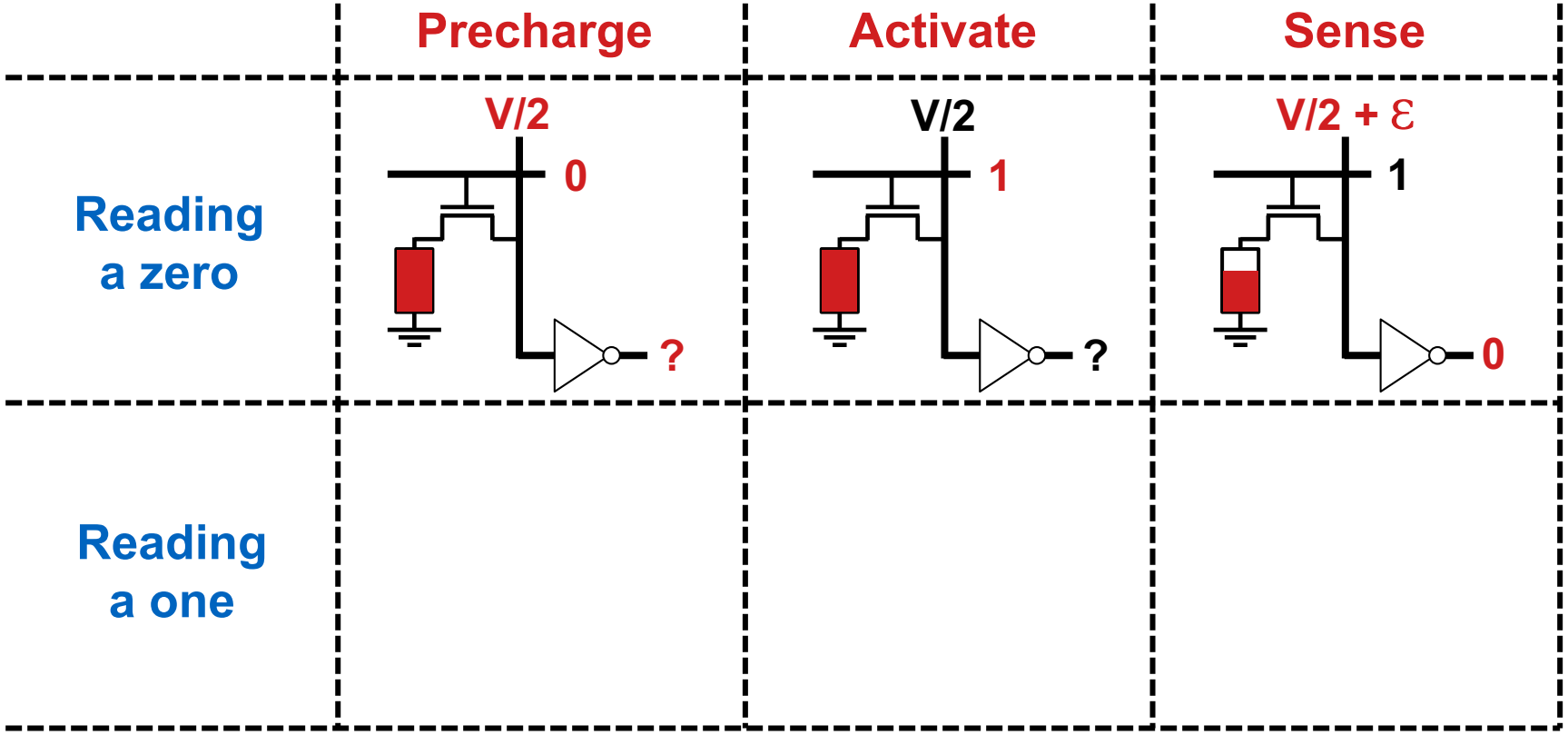

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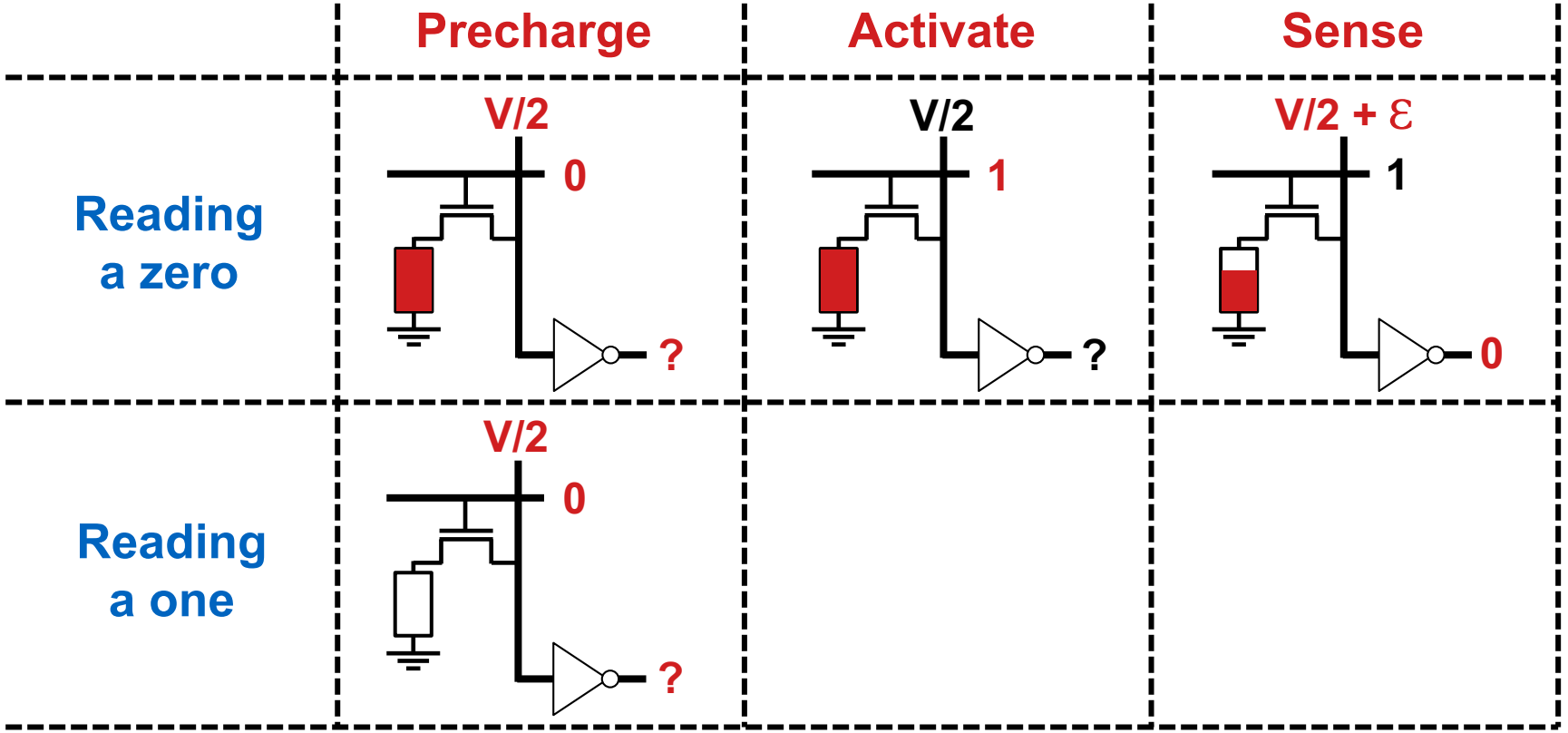

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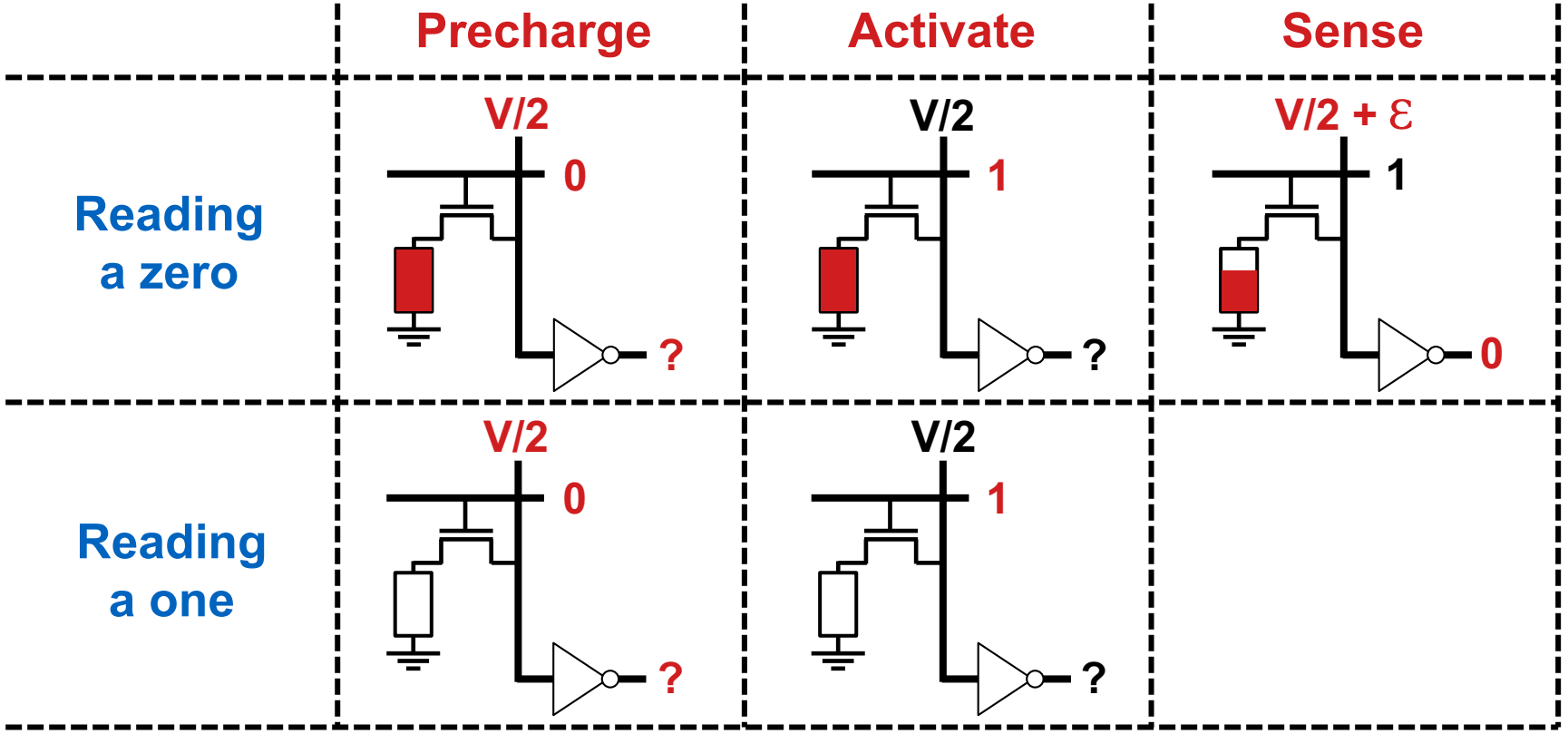

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