CACHE ARCHITECTURE

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

University of Utah

Overview

- Announcement
  - Homework 4 will be released on Oct. 30th
- This lecture
  - Cache addressing and lookup
  - Cache optimizations
    - Techniques to improve miss rate
    - Replacement policies
    - Write policies

Recall: Cache Optimizations

- How to improve cache performance?

$$AMAT = t_h + r_m \, t_p$$

- Reduce hit time (t_h)
- Improve hit rate ($1 - r_m$)
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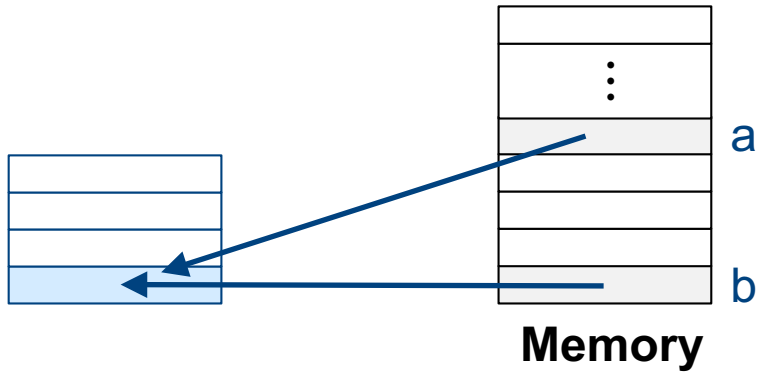
- Reduce miss penalty (t_p)
  - Multi level caches, data prefetching

Set Associative Caches

- Improve cache hit rate by allowing a memory location to be placed in more than one cache block
  - N-way set associative cache
  - Fully associative
- For fixed capacity, higher associativity typically leads to higher hit rates
  - more places to simultaneously map cache lines
  - 8-way SA close to FA in practice

```
for (i=0; i<10000; i++) {
    a++;
    b++;
}
```



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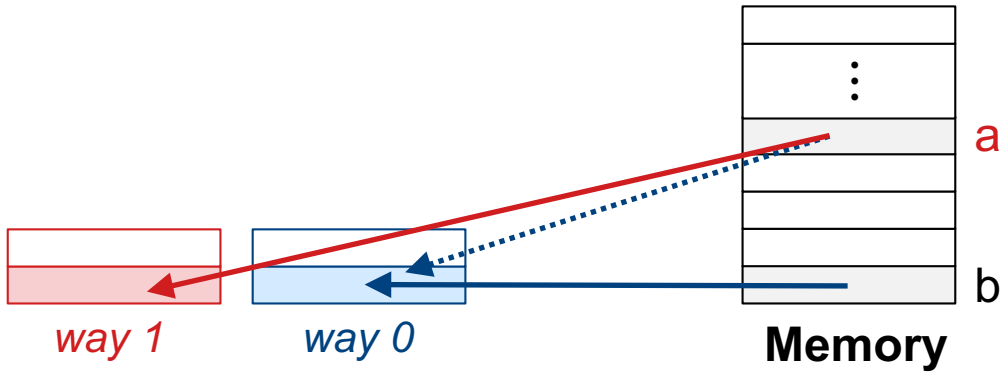
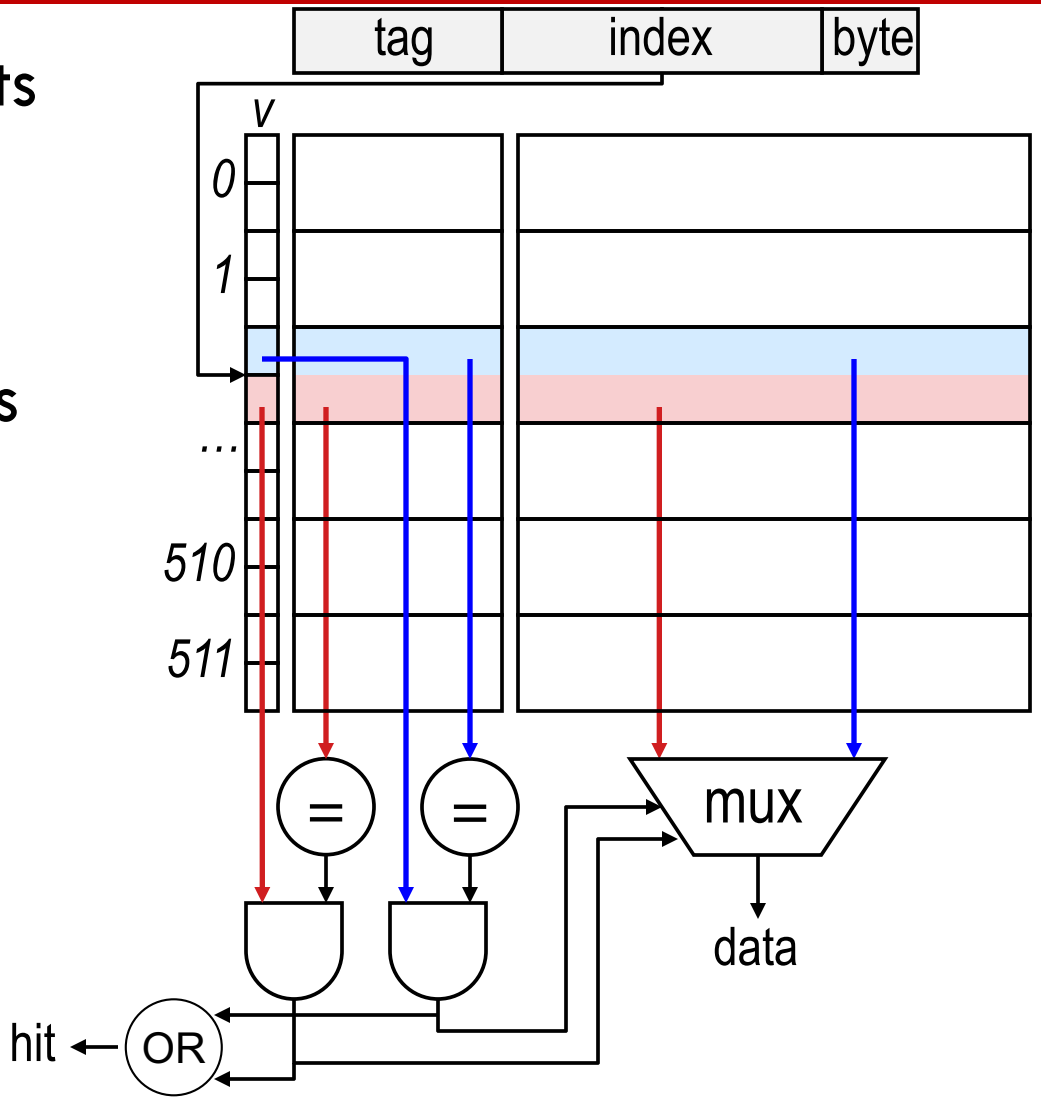


n-Way Set Associative Lookup

- Index into cache sets
- Multiple tag comparisons
- Multiple data reads
- Special cases
  - Direct mapped
    - Single block sets
  - Fully associative
    - Single set cache



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- $4GB = 2^{32}$ B → address bits = 32
- $32B = 2^{5}$ B → byte offset bits = 5
- $4MB/(4x32B) = 2^{15}$ → index bits = 15
- tag bits = 32 – 5 – 15 = 12

Cache Miss Classifications

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❑ Cold start: first access to block	❑ Cache is smaller than the program data
❑ How to improve	❑ How to improve
○ large blocks	○ large cache
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❑ Cold start: first access to block ❑ How to improve ○ large blocks ○ prefetching	❑ Cache is smaller than the program data ❑ How to improve ○ large cache	❑ Set size is smaller than mapped mem. locations ❑ How to improve ○ large cache ○ more assoc.

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- L1 miss rates
  - Local/global: 3,000/100,000 = 3%
- L2 miss rates
  - Local: 1,500/3,000 = 50%
  - Global: 1,500/100,000 = 1.5%

Cache Replacement Policies

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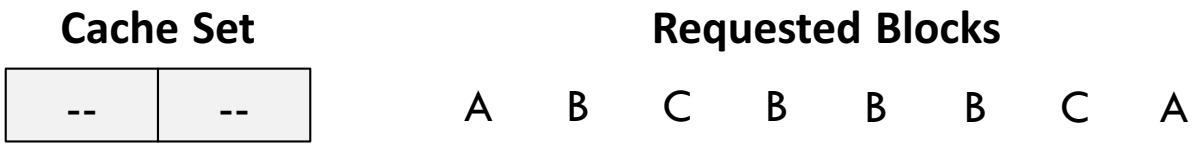

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