DYNAMIC SCHEDULING

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

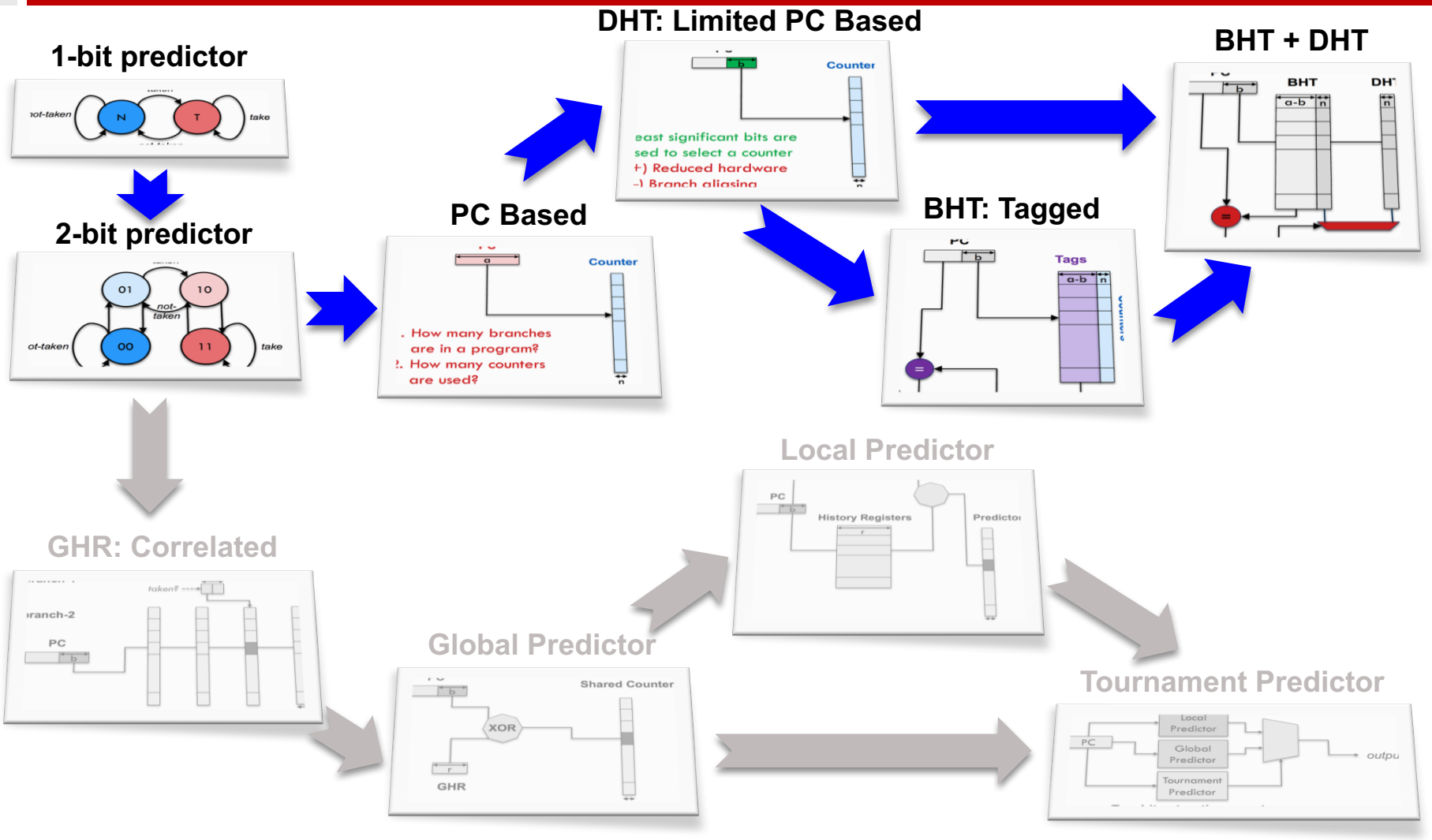
University of Utah

Overview

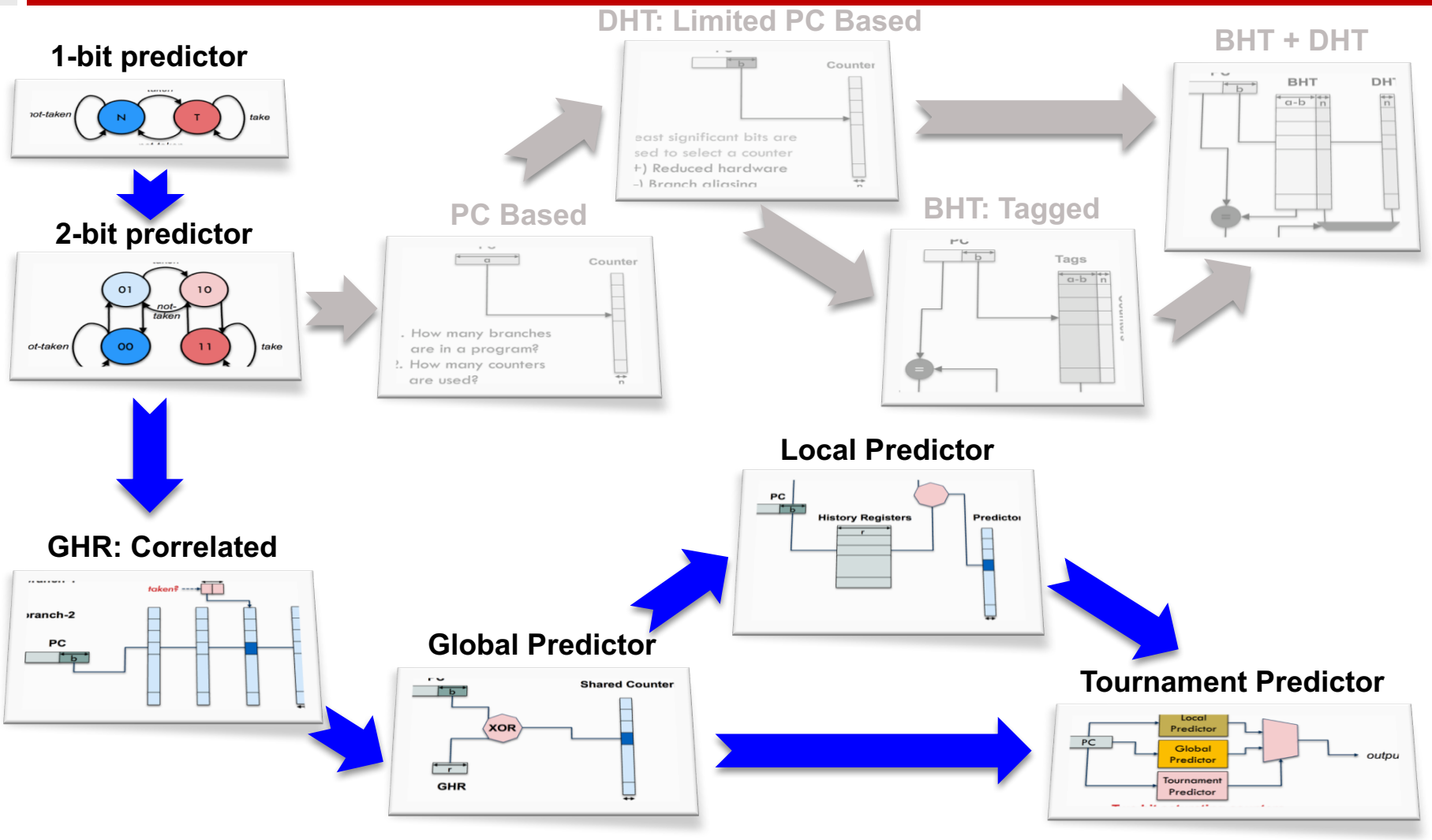
- Announcement
  - Homework 3 will be uploaded tonight (11:59PM)

- This lecture
  - Recap Branch Prediction
  - Dynamic scheduling
    - Forming data flow graph on the fly
  - Register renaming
    - Removing false data dependence
    - Architectural vs. physical registers

Recall: Branch Predictors



Recall: Branch Predictors

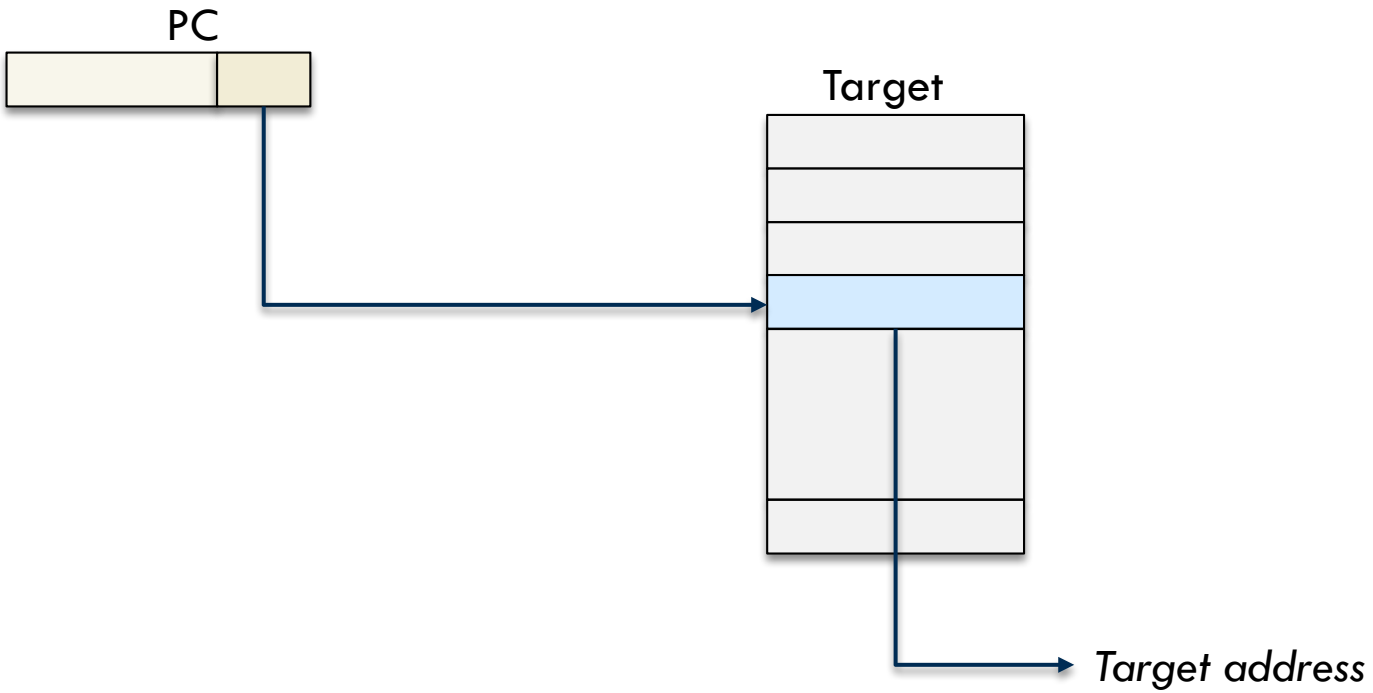


Branch Prediction Summary

- Dedicated predictor per branch
  - Program counter is used for assigning predictors to branches
- Capturing correlation among branches
  - Shift register is used to track history
- Predicting branch direction is not enough
  - Which instruction to be fetched if taken?
- Storing the target instruction can eliminate fetching
  - Extra hardware is required

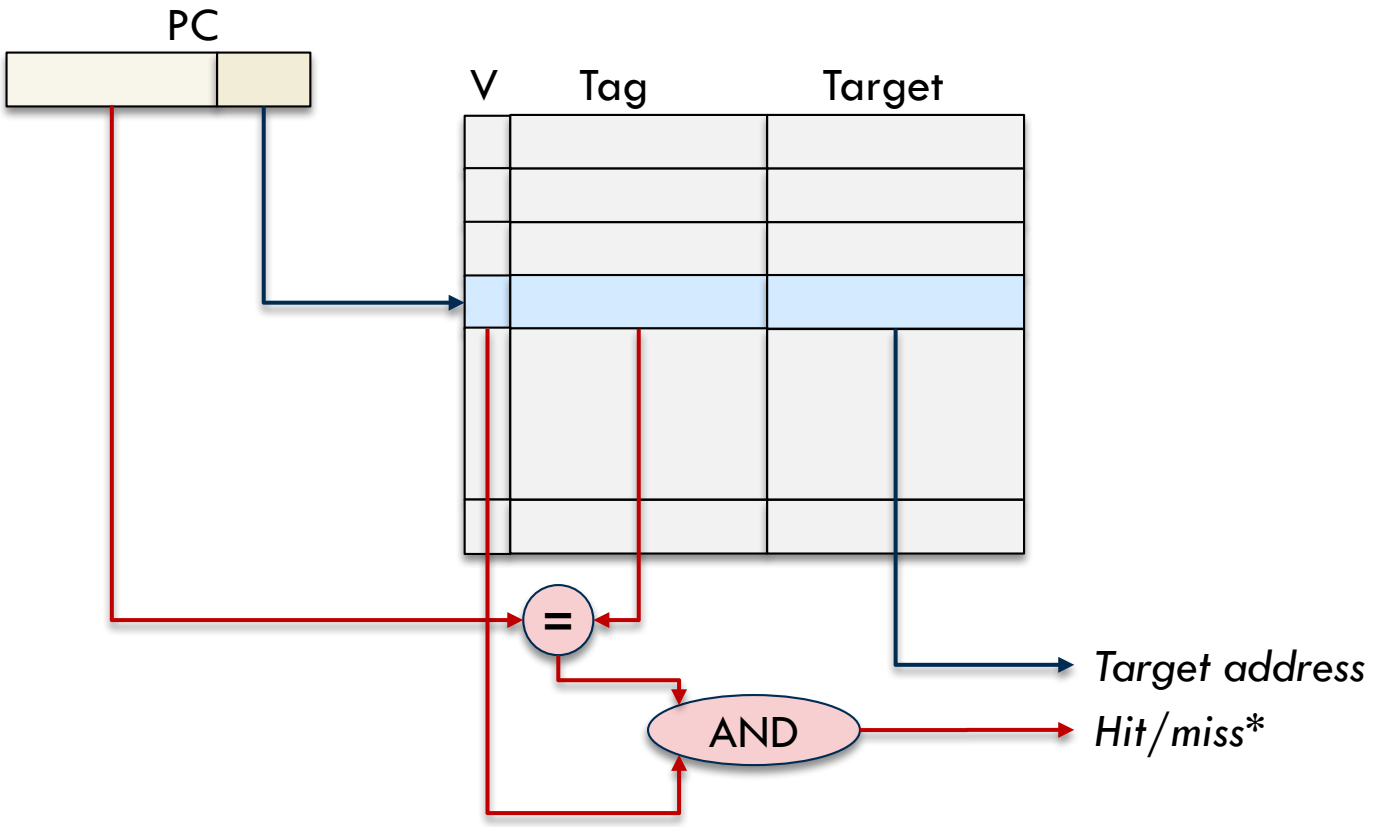
Branch Target Buffer

- Store a target address for each branch



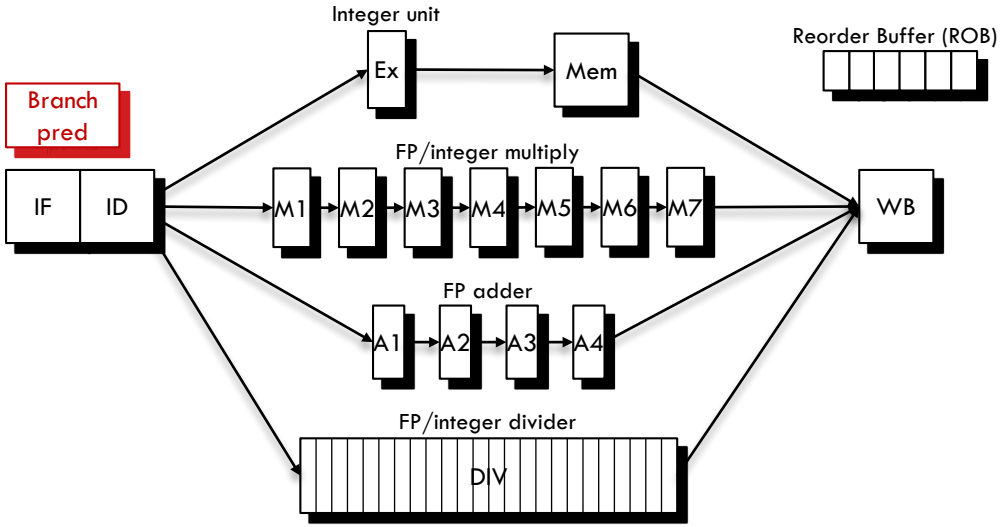
Branch Target Buffer

- Store tags and target addresses for each branch



Big Picture

- Goal: exploiting more ILP by avoiding stall cycles
  - Branch prediction can avoid the stall cycles in the frontend



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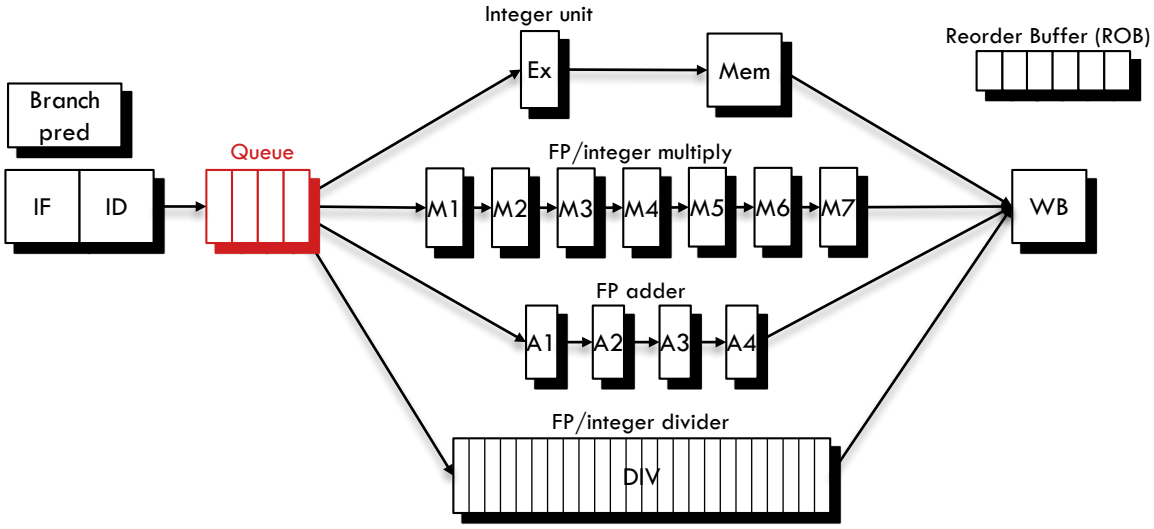
    - More instructions are sent to the pipeline



Big Picture

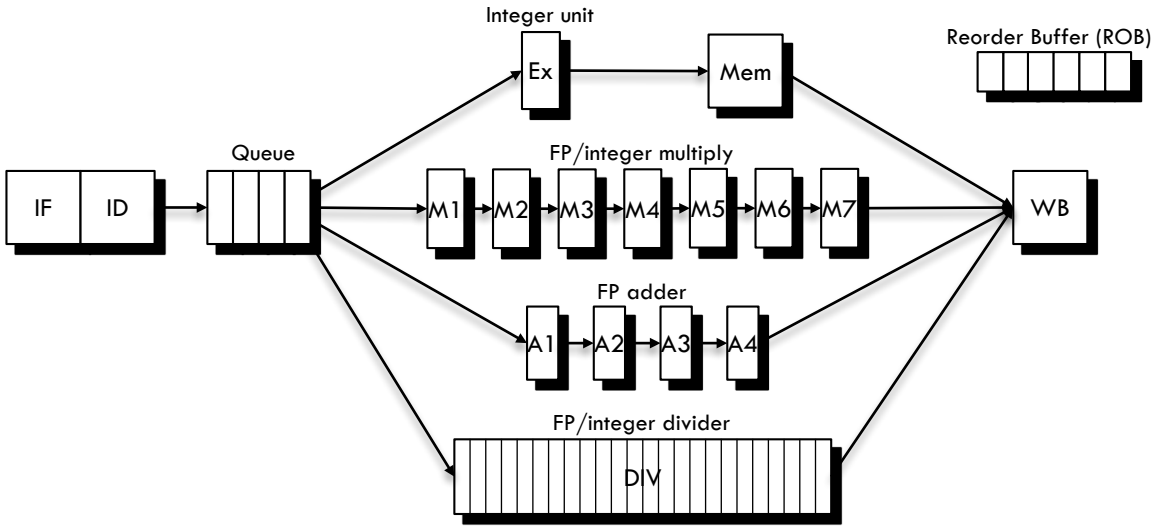
- Goal: exploiting more ILP by avoiding stall cycles
  - Branch prediction can avoid the stall cycles in the frontend
    - More instructions are sent to the pipeline
  - Instruction scheduling can remove unnecessary stall cycles in the execution/memory stage
    - Static scheduling
      - Complex software (compiler)
      - Unable to resolve all data hazards (no access to runtime details)
    - Dynamic scheduling
      - Completely done in hardware

Dynamic Scheduling

- Key idea: creating an instruction schedule based on runtime information
  - Hardware managed instruction reordering

Assembly code:

```
DIV   F1, F2, F3
ADD   F4, F1, F5
SUB   F6, F5, F7
```



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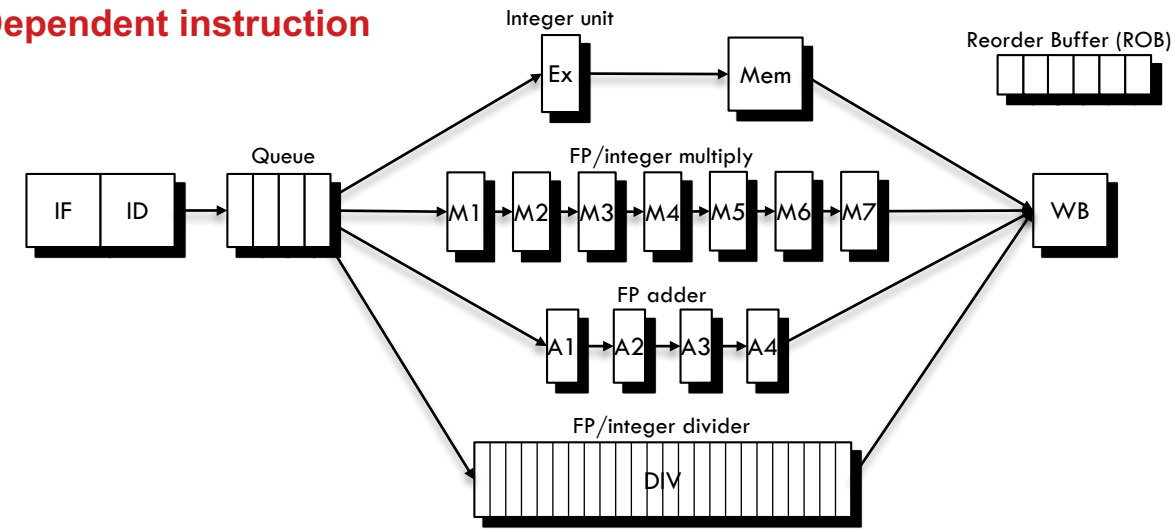
Long latency operation

Dependent instruction



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Long latency operation

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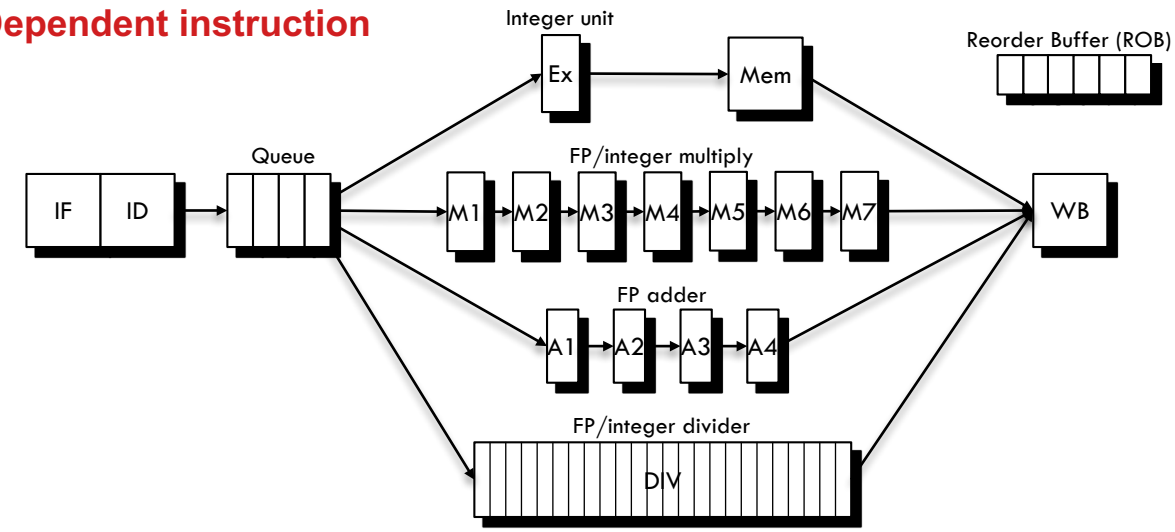
Independent instruction

Out-of-order execution?



Dynamic Scheduling

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  - Instructions are executed in data flow order

Program code

```
        ADDI  R1, R0, #1
        ADDI  R2, R0, #4
loop:   ADD   R3, R3, R2
        ADDI  R2, R2, #-1
        BNEQ R2, R1, next
        ADD   R4, R4, R3
next:   BNEQ R2, R0, loop
```

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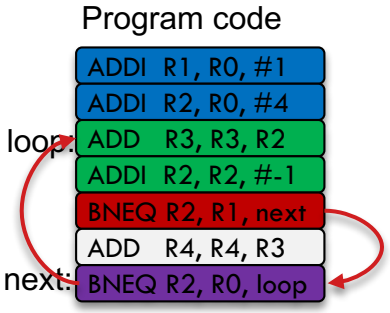

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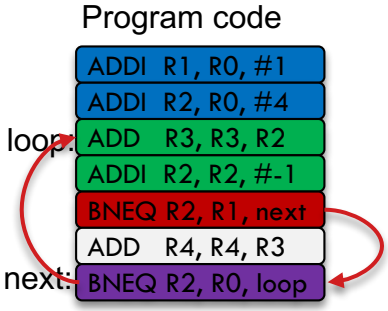

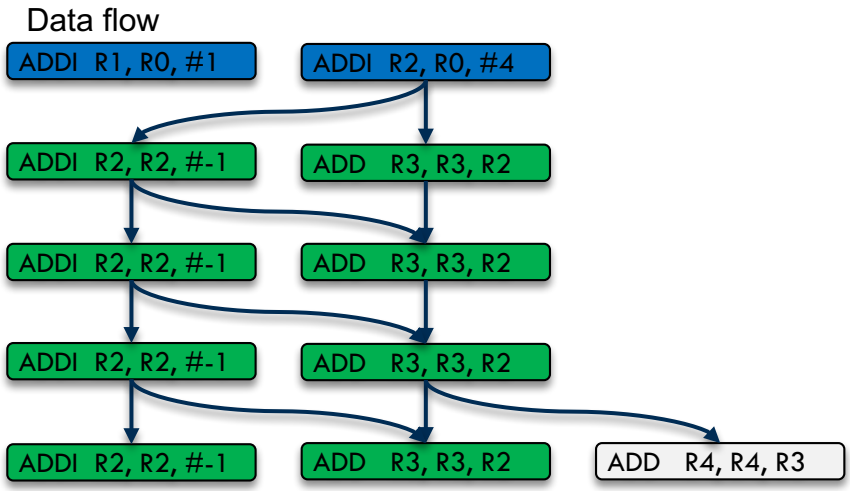

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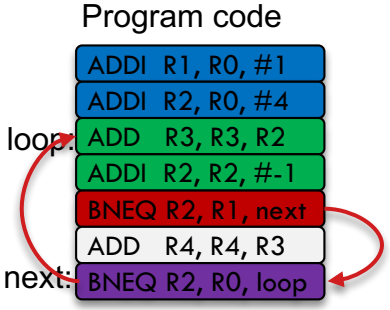

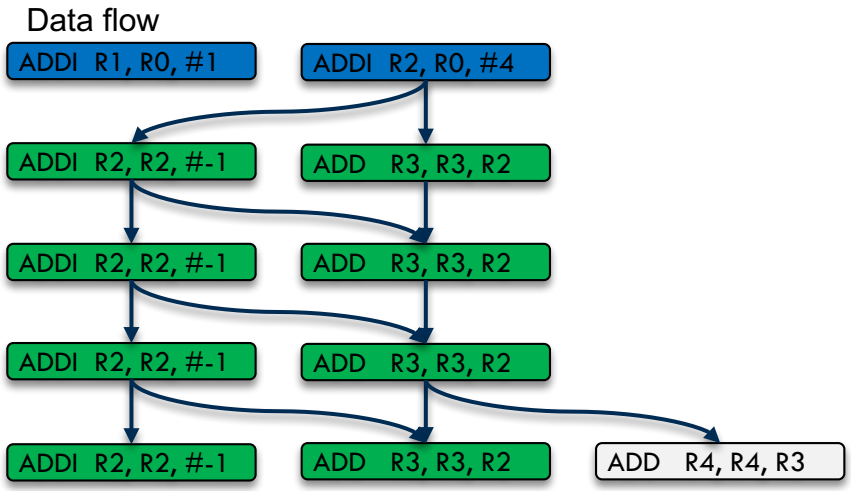

How to form data flow graph on the fly?

Register Renaming

- Eliminating WAR and WAW hazards
  - Change the mapping between architectural registers and physical storage locations

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DIV   F1, F2, F3
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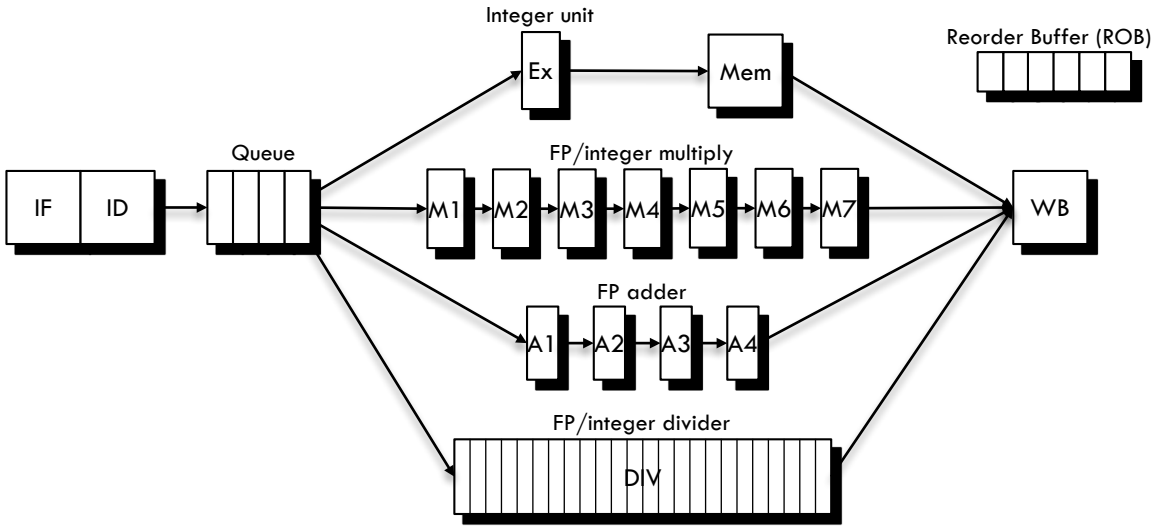

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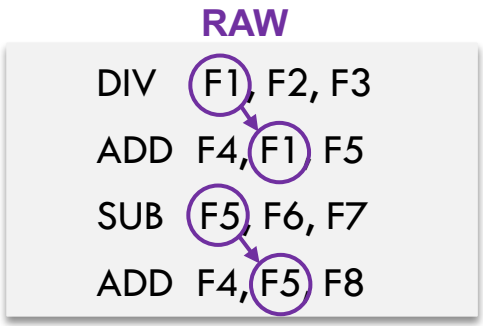

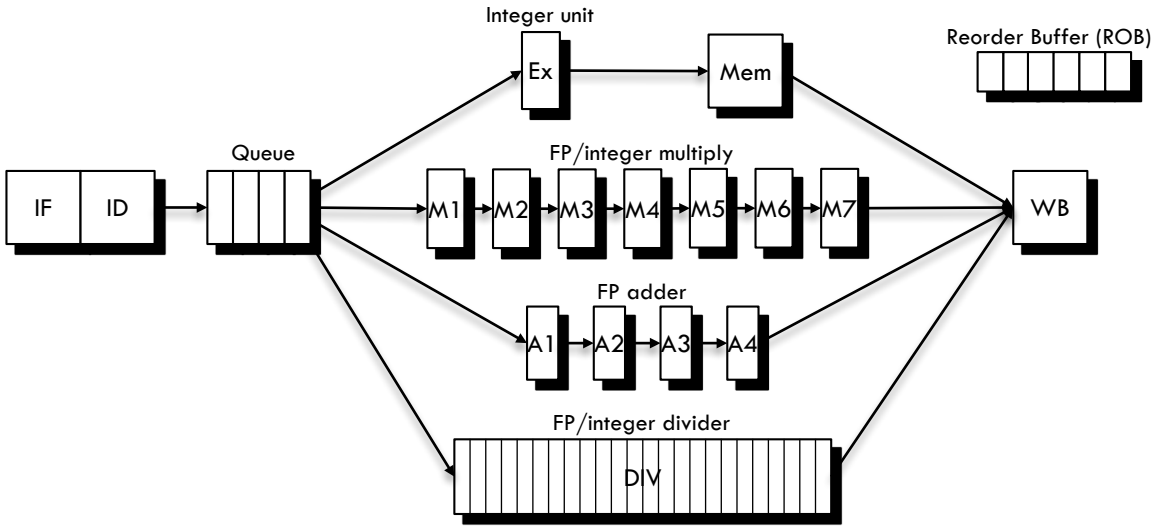

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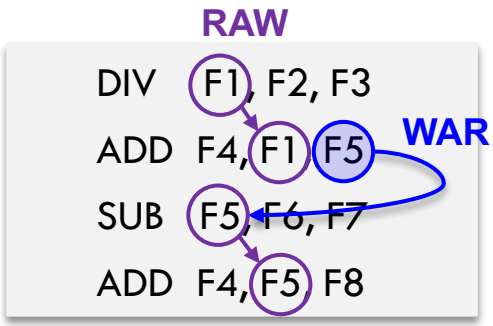

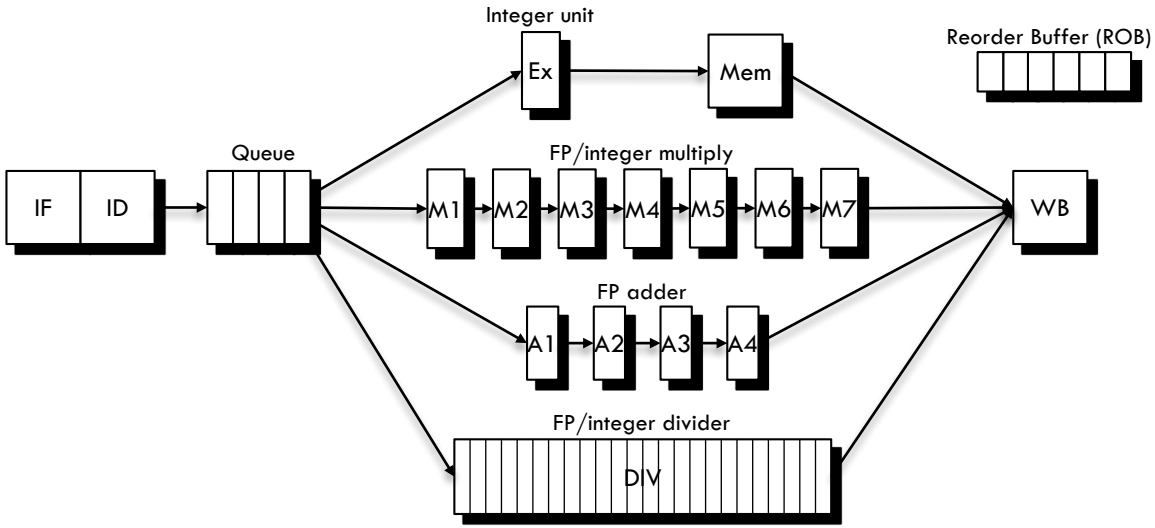

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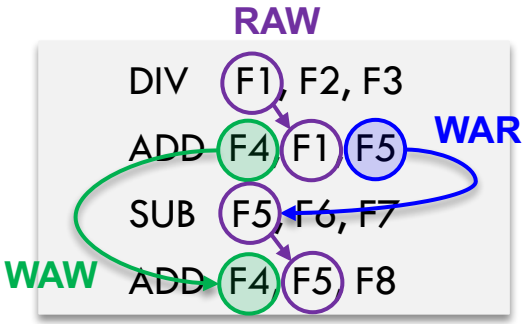

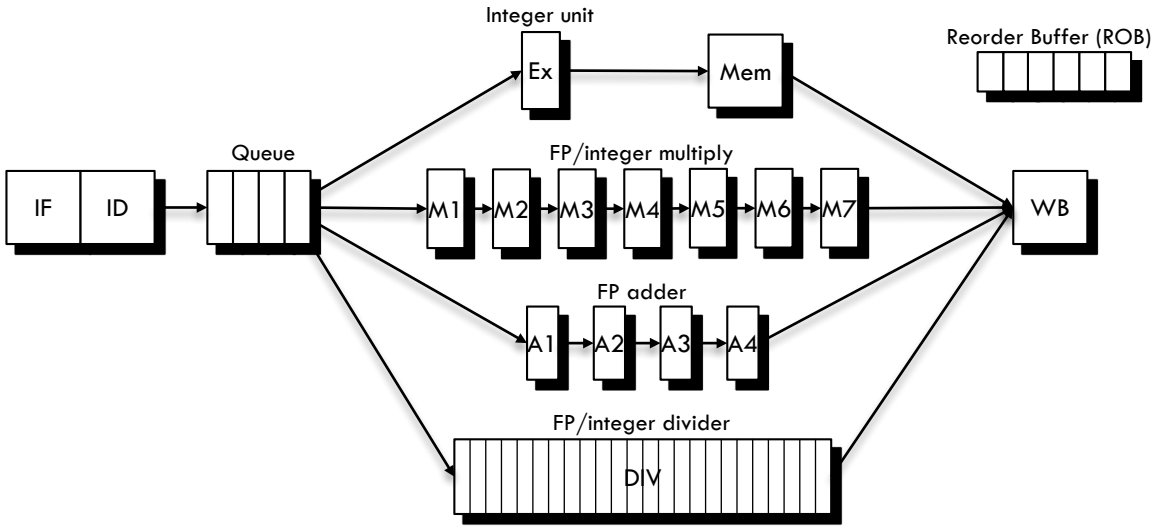

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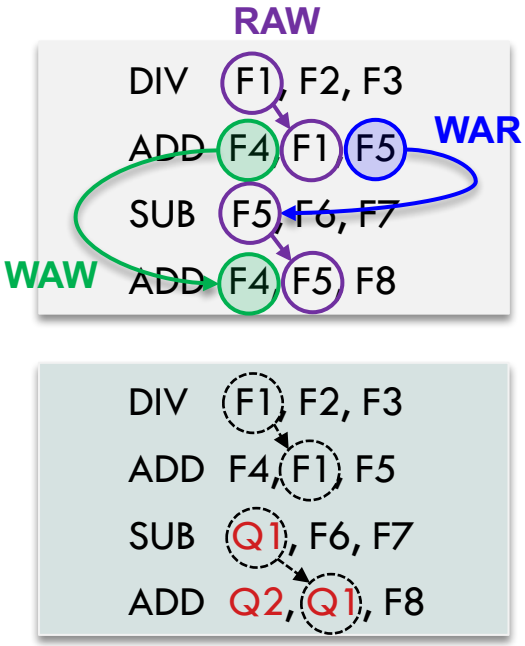

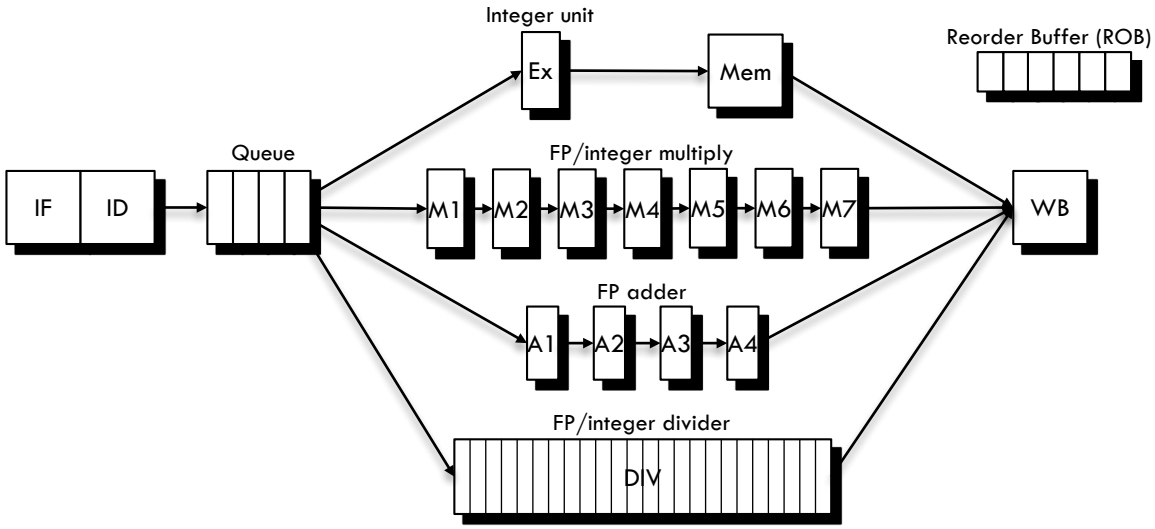

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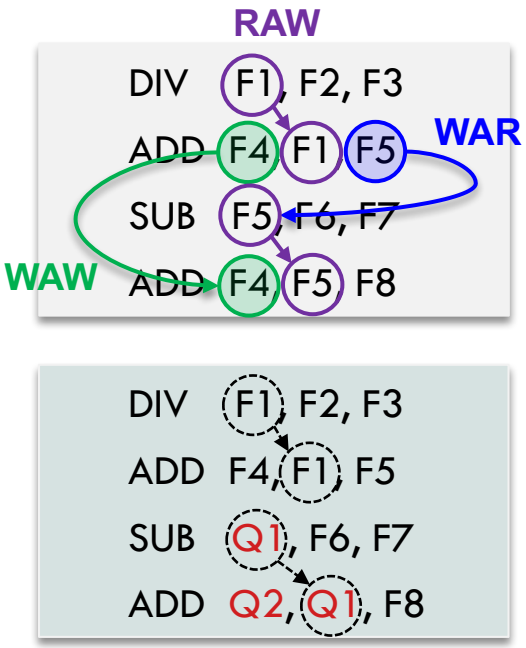
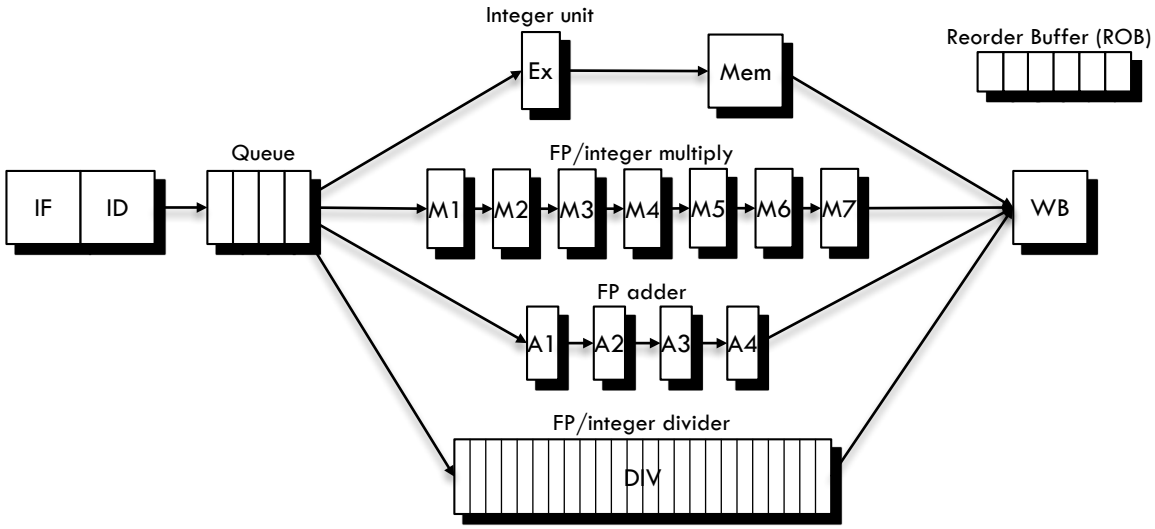


WAR and WAW hazards can be removed using more registers



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- Eliminating WAR and WAW hazards
  - 1. allocate a free physical location for the new register
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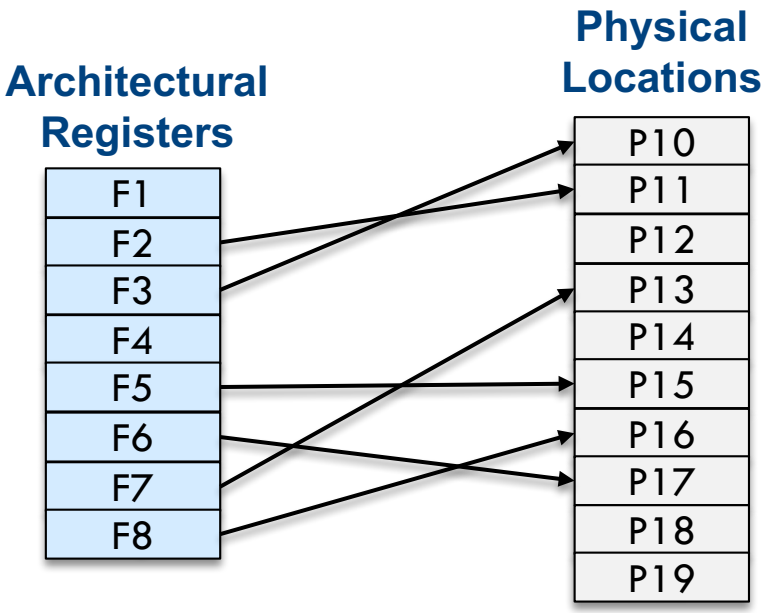

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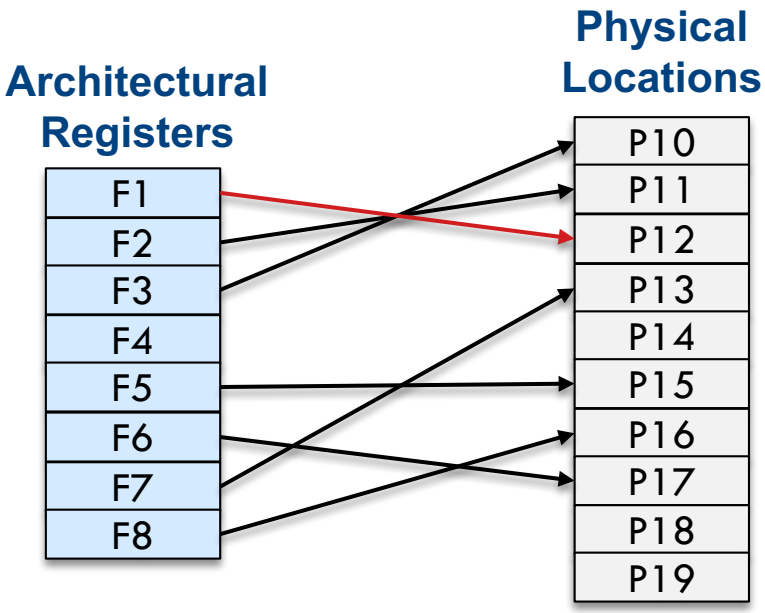
```
DIV   P12, P11, P10
```



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```
DIV   P12, P11, P10
ADD   P14, P12, P15
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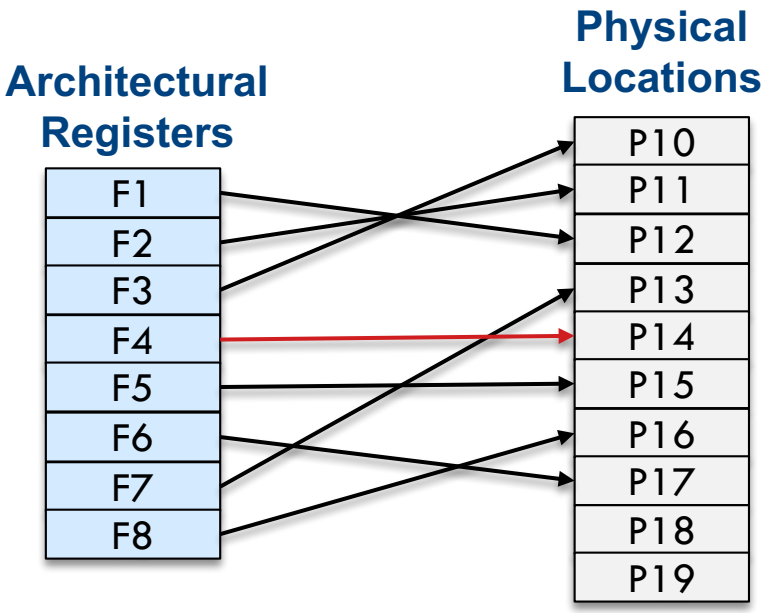

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DIV   P12, P11, P10
ADD   P14, P12, P15
SUB   P19, P17, P13
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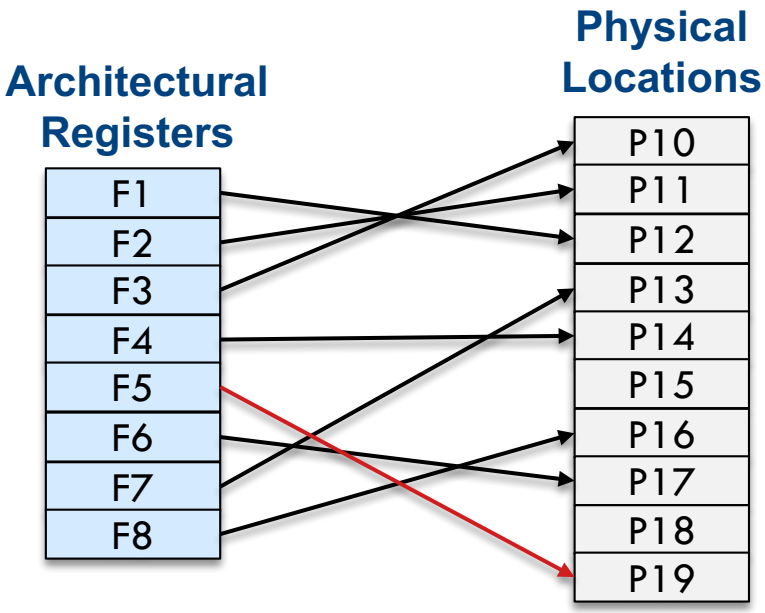

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ADD   P14, P12, P15
SUB   P19, P17, P13
ADD   P18, P19, P16
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