INTRODUCTION AND LOGISTICS

Mahdi Nazm Bojnordi

Assistant Professor

School of Computing

University of Utah

THE UNIVERSITY OF UTAH

CS/ECE 6810: Computer Architecture

Overview

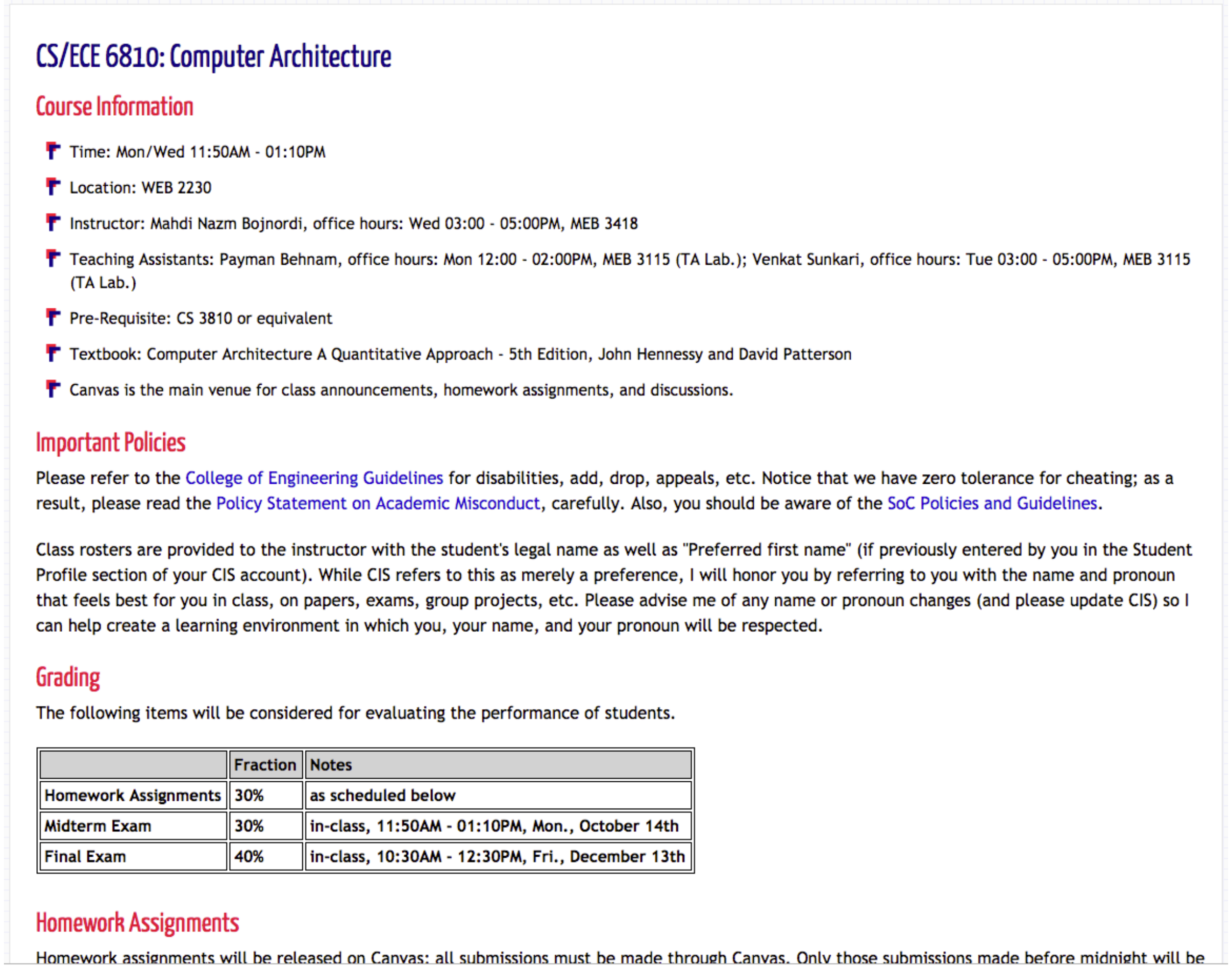
- This lecture
  - Instructor
  - Teaching assistants
  - Course resources and requirements
  - Academic integrity
  - Computer architecture
  - Trends and challenges

Instructor

- Mahdi Nazm Bojnordi
  - Assistant Professor of School of Computing
  - PhD degree in Electrical Engineering
  - Personal webpage: http://www.cs.utah.edu/~bojnordi/
- Research in Computer Architecture
  - Novel Memory Technologies
  - Energy-Efficient Hardware Accelerators
  - Research Lab. (MEB 3383)
    - Open positions are available for motivated students!
- Office Hours (MEB 3418)
  - Wed. 3:00-5:00PM
- Class webpage: http://www.cs.utah.edu/~bojnordi/classes/6810/f19/

Webpage

- Please visit online



CS/ECE 6810: Computer Architecture

Course Information

- Time: Mon/Wed 11:50AM - 01:10PM
- Location: WEB 2230
- Instructor: Mahdi Nazm Bojnordi, office hours: Wed 03:00 - 05:00PM, MEB 3418
- Teaching Assistants: Payman Behnam, office hours: Mon 12:00 - 02:00PM, MEB 3115 (TA Lab.); Venkat Sunkari, office hours: Tue 03:00 - 05:00PM, MEB 3115 (TA Lab.)
- Pre-Requisite: CS 3810 or equivalent
- Textbook: Computer Architecture A Quantitative Approach - 5th Edition, John Hennessy and David Patterson
- Canvas is the main venue for class announcements, homework assignments, and discussions.

Important Policies

Please refer to the College of Engineering Guidelines for disabilities, add, drop, appeals, etc. Notice that we have zero tolerance for cheating; as a result, please read the Policy Statement on Academic Misconduct, carefully. Also, you should be aware of the SoC Policies and Guidelines.

Class rosters are provided to the instructor with the student's legal name as well as "Preferred first name" (if previously entered by you in the Student Profile section of your CIS account). While CIS refers to this as merely a preference, I will honor you by referring to you with the name and pronoun that feels best for you in class, on papers, exams, group projects, etc. Please advise me of any name or pronoun changes (and please update CIS) so I can help create a learning environment in which you, your name, and your pronoun will be respected.

Grading

The following items will be considered for evaluating the performance of students.

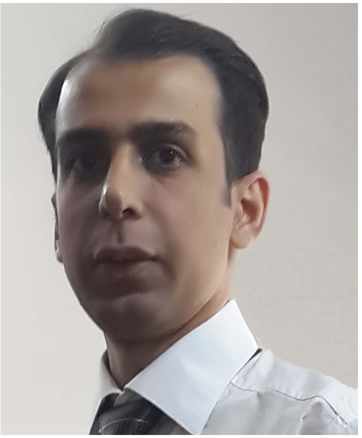
	Fraction	Notes
Homework Assignments	30%	as scheduled below
Midterm Exam	30%	in-class, 11:50AM - 01:10PM, Mon., October 14th
Final Exam	40%	in-class, 10:30AM - 12:30PM, Fri., December 13th

Homework Assignments

Homework assignments will be released on Canvas; all submissions must be made through Canvas. Only those submissions made before midnight will be

Teaching Assistants

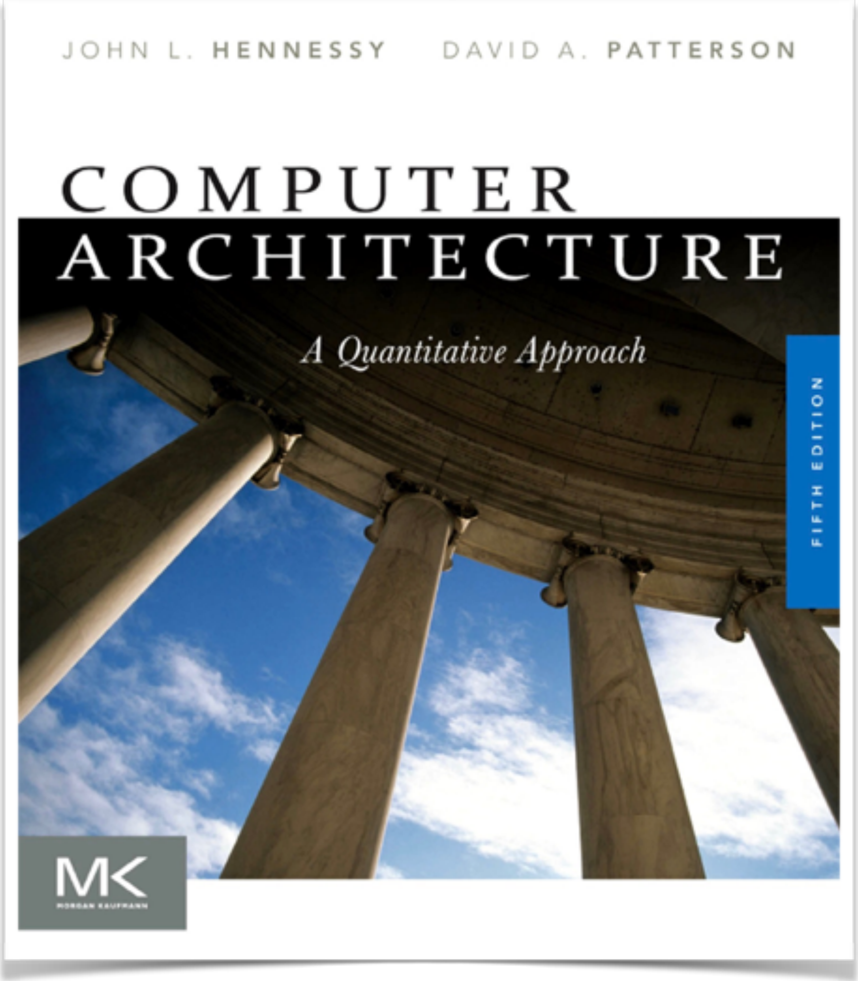
- Payman Behnam
  - Email: paymanbehnam@gmail.com
  - Office Hours: Mon. 12:00-2:00PM
  - MEB 3115 (TA Lab.)



- Venkatrajreddy Sunkari
  - Email: venkatrajreddy.sunkari@utah.edu
  - Office Hours: Tue. 3:00-5:00PM
  - MEB 3115 (TA Lab.)

Resources and Requirements

- Textbook: Computer Architecture A Quantitative Approach - 5th Edition, John Hennessy and David Patterson
- Pre-requisite: CS/ECE 3810 or equivalent



Course Expectation

- We use Canvas for homework submissions, grades, and homework announcements.
- Grading

	Fraction	Notes
Assignments	30%	homework assignments
Midterm Exam	30%	Monday, October 15th
Final Exam	40%	Thursday, December 13th
Class Participation	--%	Questions and answers in class

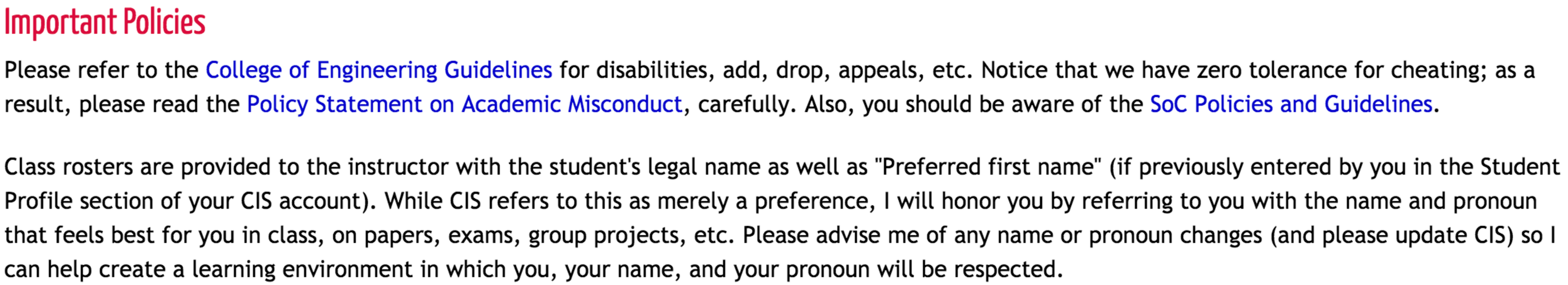
Homework Assignments

- Homework assignments will be released on Canvas; all submissions must be made through Canvas.
- Only those submissions made before midnight will be accepted.
  - Important: Please verify your uploaded file before midnight.
- Any late submission will be considered as no submission.

	Release Date	Submission Deadline
Homework 1	August 28th	September 4th
Homework 2	September 11th	September 18th
Homework 3	September 25th	October 2nd
Homework 4	October 30th	November 6th
Homework 5	November 13th	November 20th

Academic Integrity

- Do NOT cheat!!
  - Please read the Policy Statement on Academic Misconduct, carefully.
  - We have no tolerance for cheating
- Also, read to the College of Engineering Guidelines for disabilities, add, drop, appeals, etc.



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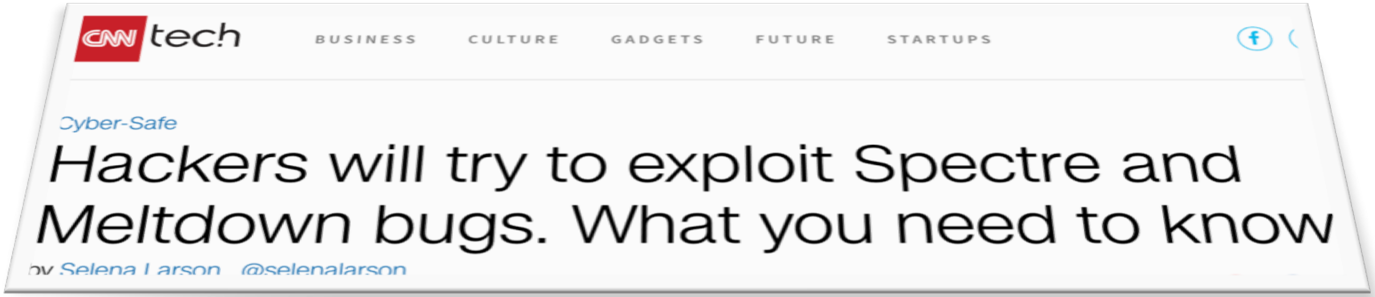
Why CS/ECE 6810?

- Need another qualifier/graduation requirement?
- You plan to become a Computer Architect?
- Understand what is inside a modern processor?
- Want to use the knowledge from this course in your own field of study?
- Understand the technology trends and recent developments for future computing?
- …

Why CS/ECE 6810?

- Better understanding of today’s computing problems
  - Security flaw: Spectre and Meltdown

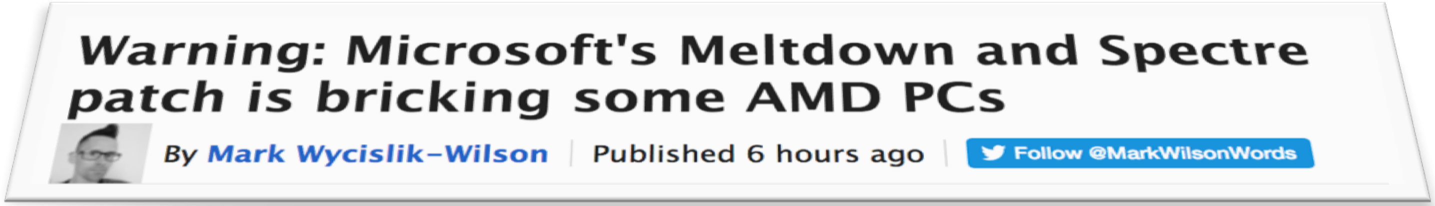


Cyber-Safe

Hackers will try to exploit Spectre and Meltdown bugs. What you need to know

by Selena Larson @selenalarson

  - How to fix?



Warning: Microsoft's Meltdown and Spectre patch is bricking some AMD PCs

By Mark Wycislik-Wilson | Published 6 hours ago

Estimated Class Schedule

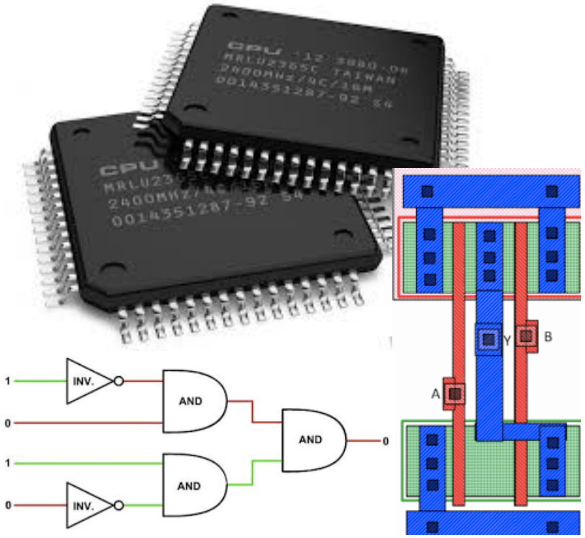
- Processor Core
  - Introduction and Performance Metrics
  - Instruction Set Architecture and Pipelining
  - Instruction-Level Parallelism
  - Compiler Optimization
  - Dynamic Instruction Scheduling
- Memory System
  - Cache Architecture
  - Virtual Memory
  - Main Memory and DRAM
  - Data Parallel Processors

What is Computer Architecture?

- Computer systems are everywhere …

What is Computer Architecture?

□ What is inside modern processors …



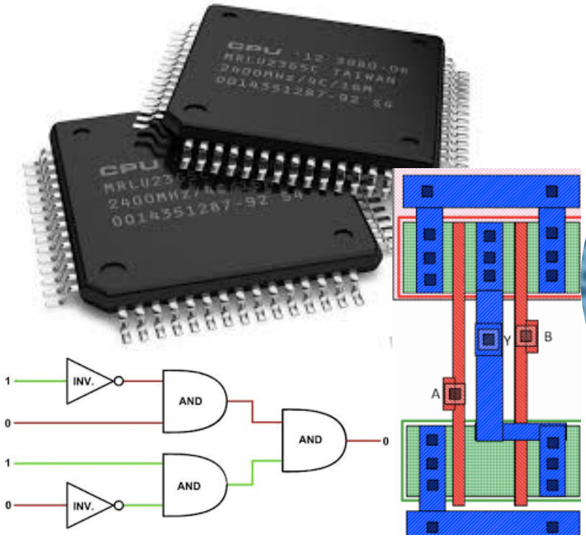
?

**VLSI Circuits
Hardware Implementation**

**Software Applications
OS and Compiler**

What is Computer Architecture?

- Computer architecture is the glue between software and VLSI implementation



ISA, µarchitecture , system Architecture

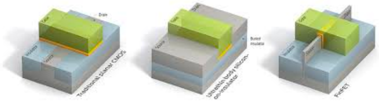
VLSI Circuits
Hardware Implementation

Software Applications
OS and Compiler

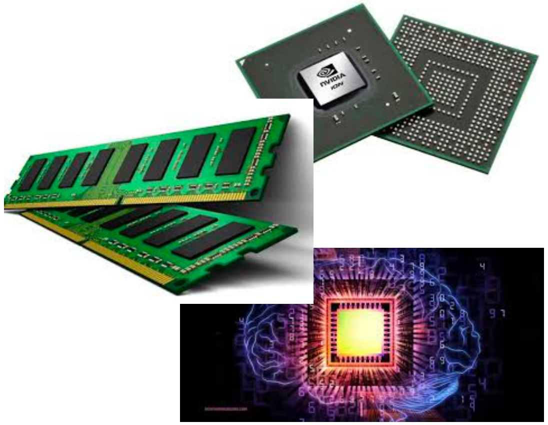
What is Computer Architecture?

- Architects

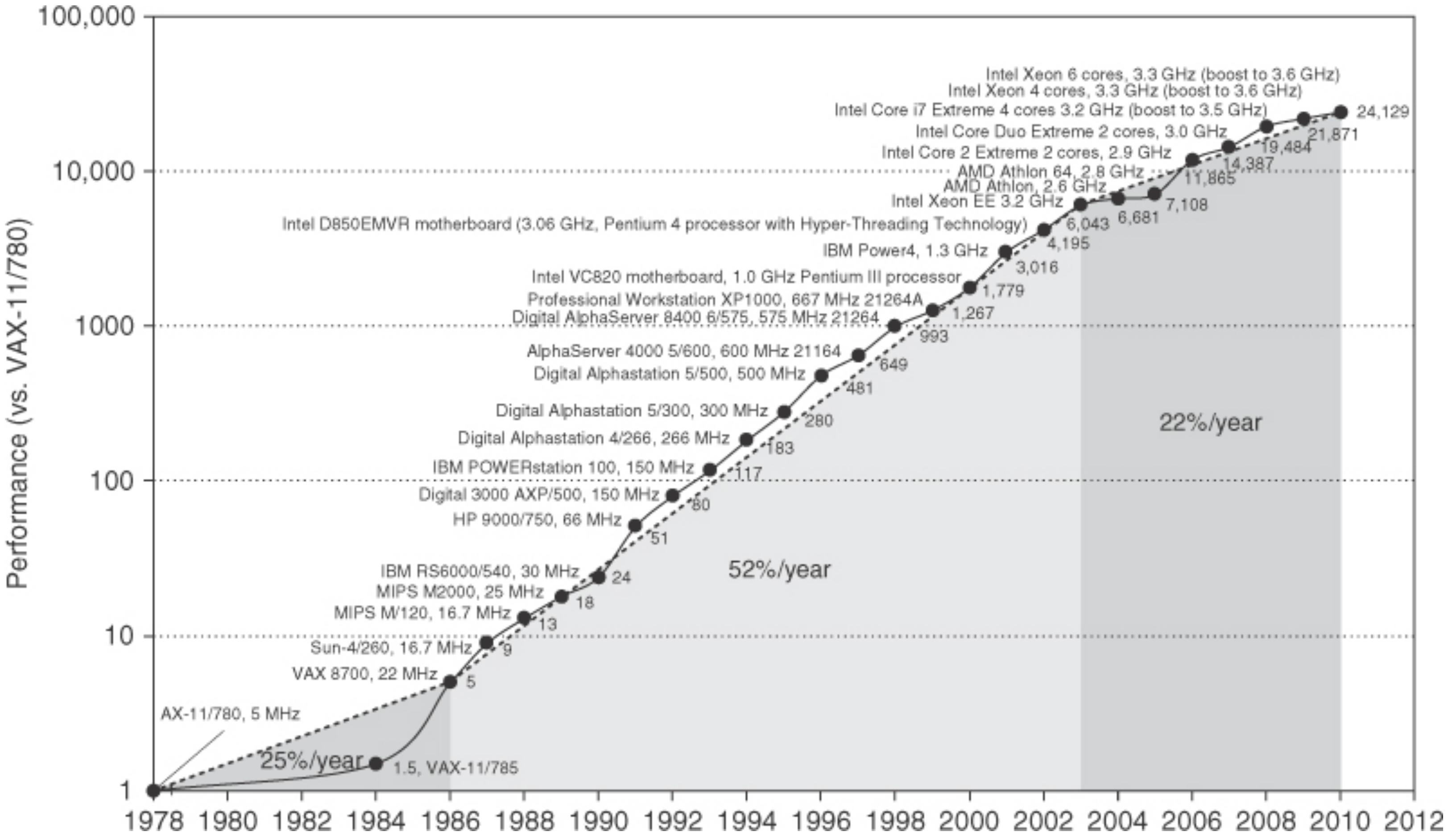
- Computer Architects



Computer Architects



Growth in Processor Performance



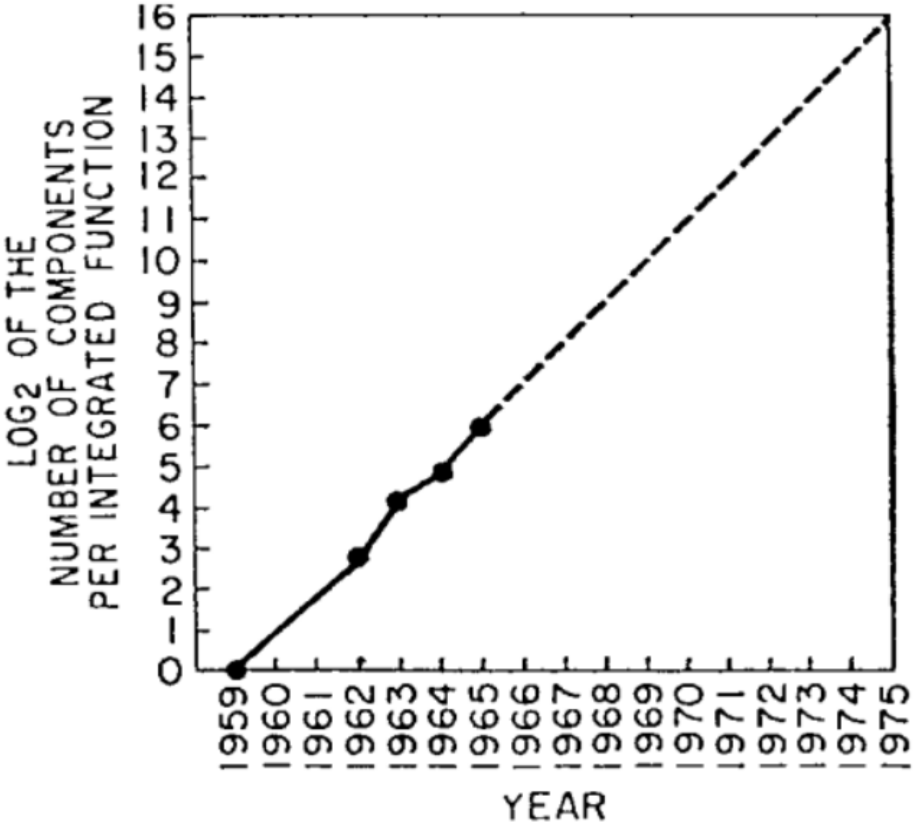
Source: Hennesy & Patterson Textbook

Growth in Processor Performance

- Main sources of the performance improvement
  - Enhanced underlying technology (semiconductor)
    - Faster and smaller transistors (Moore’s Law)
  - Improvements in computer architecture
    - How to better utilize the additional resources to gain more power savings, functionalities, and processing speed.

Moore's Law

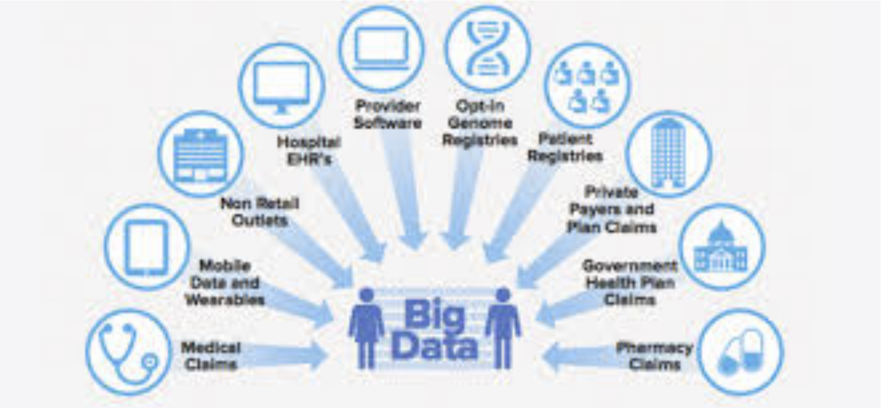
- Moore's Law (1965)
  - Transistor count doubles every year
- Moore's Law (1975)
  - Transistor count doubles every two years

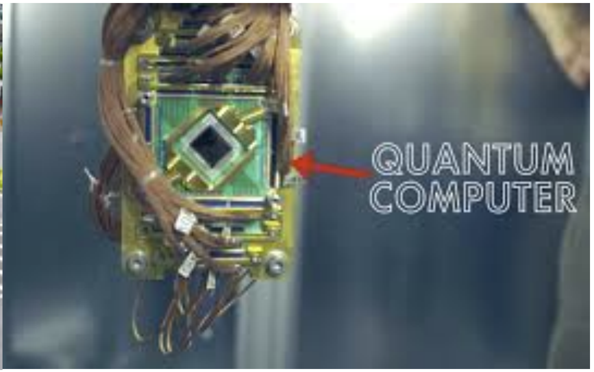


Source: G.E. Moore, "Cramming more components onto integrated circuits," 1965

Why study computer architecture?

- Do the conventional computers last forever?
  - New challenges
  - New forms of computing



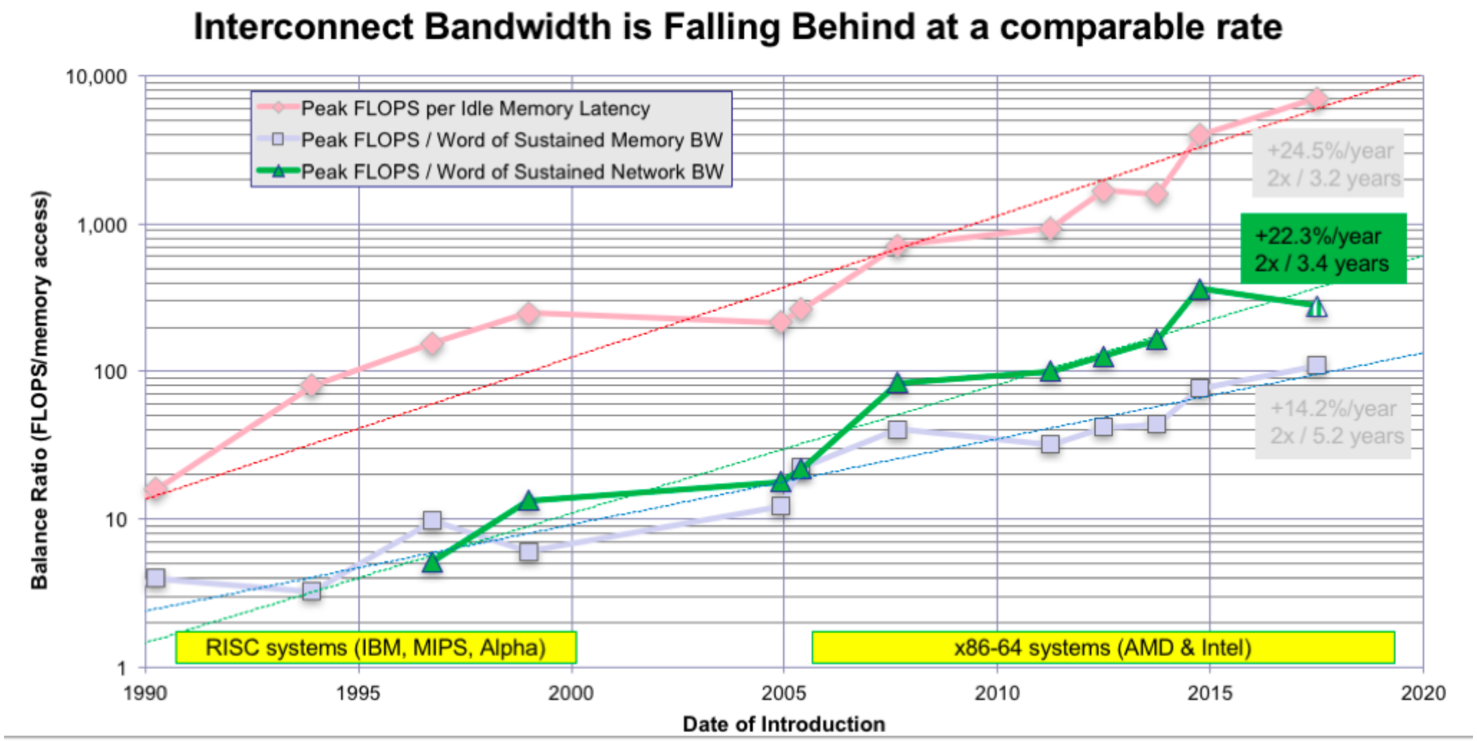


What are New Challenges?

- Resources (transistors) on a processor chip?
  - Not really, billions of transistors on a single chip.
- Can we use all of the transistors?
  - Due to energy-efficiency limitations, only a fraction of the transistor can be turned on at the same time!
- Who is affected?
  - Server computers by the peak power
  - Mobile and wearables due to energy-efficiency

What are New Challenges?

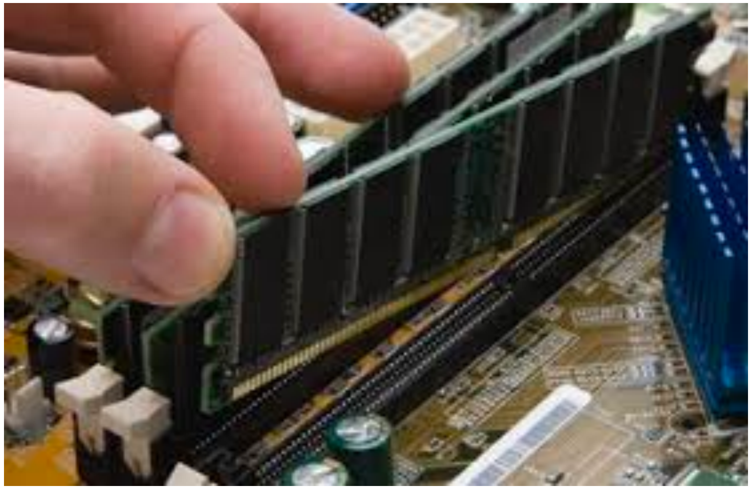
- Bandwidth optimization becomes a primary goal for memory design (Bandwidth Wall!)



What are New Challenges?

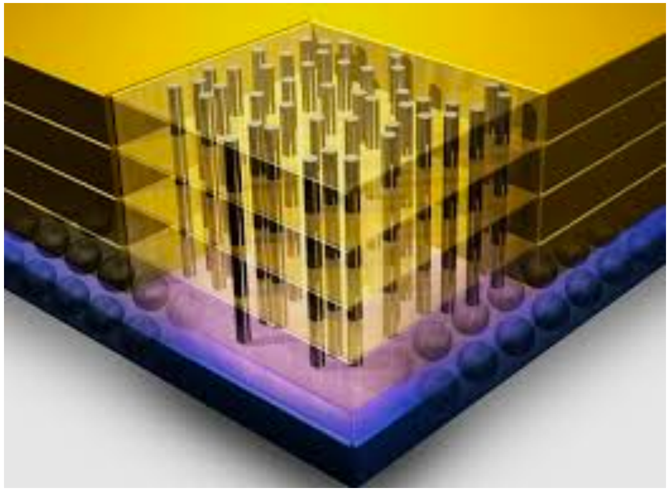
- Can in-package memory solve the problem?

Off-chip Memory



Lower Bandwidth
Lower Costs

3D Stacked Memory



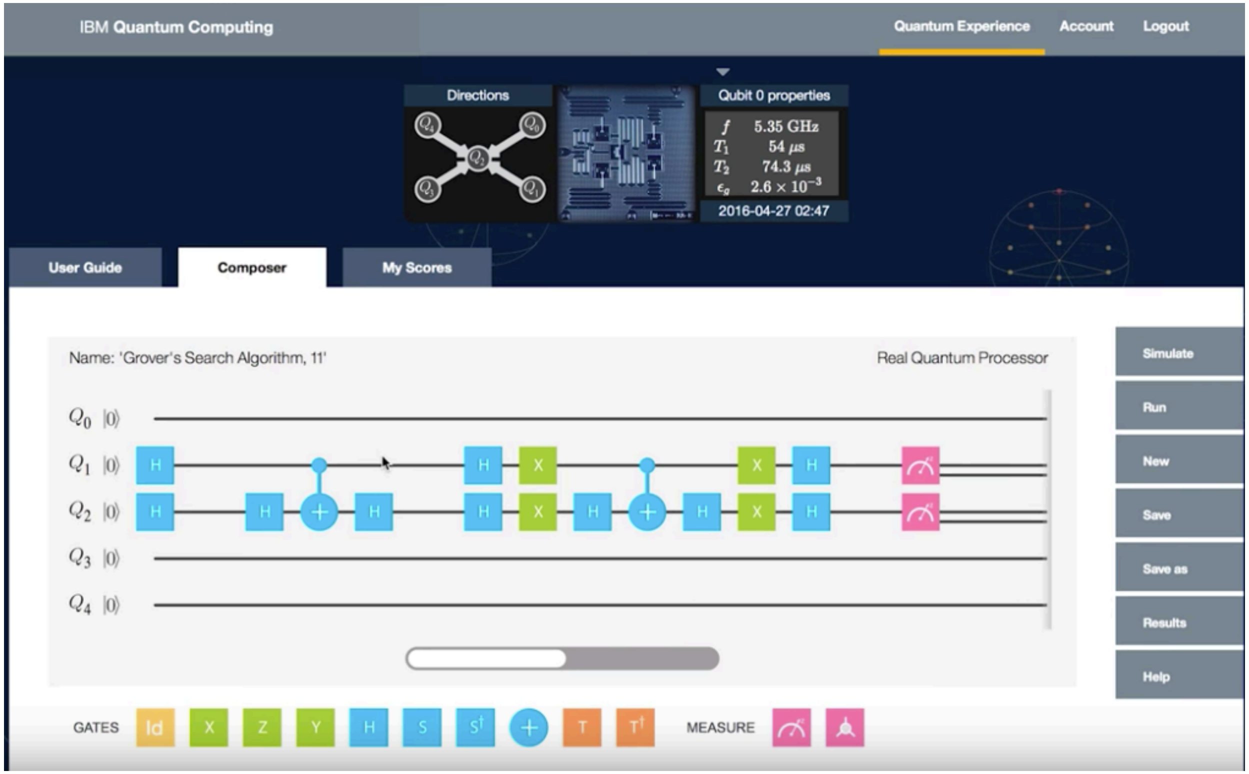
Higher Bandwidth
Higher Costs

What are New Challenges?

- Protecting data against side channel attacks is a serious need
- Performance in the past 40 years increased
  - hardware speculation to exploit more instruction level parallelism
  - shared memories to facilitate thread-level parallelism
- What about security?
  - https://meltdownattack.com/

Unconventional Computing Systems

- How to program a Quantum computer?
  - Qbit vs. bit



Qubit 0 properties

f 5.35 GHz

T_1 54 μs

T_2 74.3 μs

ϵ_g 2.6×10^{-3}

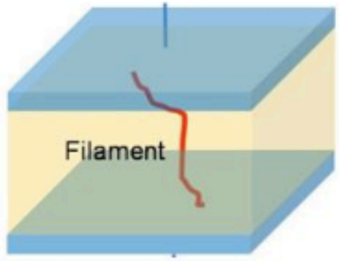
2016-04-27 02:47

Name: 'Grover's Search Algorithm, 11'

Real Quantum Processor

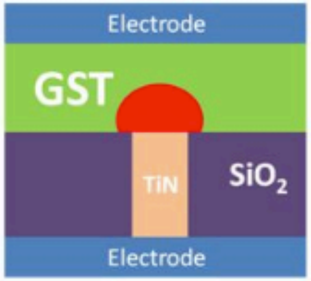
Emerging Non-volatile Memories

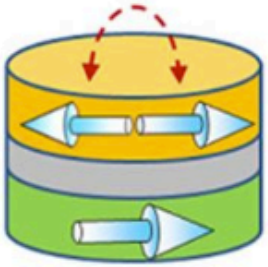
- Use resistive states to represent data
  - Can we build non-von Neumann machines?
    - In-Memory and In-situ computers



RRAM

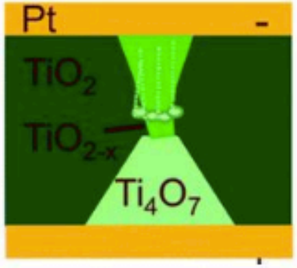
PCM





STT MRAM

CBRAM


Pt
-
TiO$_2$
TiO$_{2-x}$
Ti$_4$O$_7$