INTRODUCTION AND LOGISTICS

Mahdi Nazm Bojnordi
Assistant Professor
School of Computing
University of Utah
Overview

- This lecture
  - Instructor
  - Teaching assistants
  - Course resources and requirements
  - Academic integrity
  - Computer organization
  - Trends and challenges
Instructor

- Mahdi Nazm Bojnordi
  - Assistant Professor of School of Computing
  - PhD degree in Electrical Engineering
  - Personal webpage: http://www.cs.utah.edu/~bojnordi/

- Research in Computer Architecture
  - Novel Memory Technologies
  - Energy-Efficient Hardware Accelerators
  - Research Lab. (MEB 3383)
    - Open positions for research are available!

- Office Hours (MEB 3418)
  - Please email me for an appointment

- Class webpage: http://www.cs.utah.edu/~bojnordi/classes/3810/s19/
CS/EEC 3810: Computer Organization

Course Information
- Time: Tue/Thu 09:10AM - 10:30AM
- Location: WEB 1104
- Instructor: Nabil Nazmi, email: lastname@cs.utah.edu, office hours: email me for appointment, WEB 314B
- Teaching Assistants: Sumanth Geraparthi, email: sgeraparthi@cs.utah.edu, office hours: TBD; Lin Jia, email: Lin.Jia@utah.edu, office hours: TBD; Jacquelin Tawney, email: jettawney@gmail.com, office hours: TBD; Taylor Smith, email: tsayne@cs.utah.edu, office hours: TBD
- TAs will be available in the CAD Lab during their office hours. Please use the TA Queue to get in line.
- Pre-Requisites: Knowledge of structured programming languages such as C/Java
- Canvas is the main venue for class announcements, homework assignments, and discussions.

Important Policies
Please refer to the College of Engineering Guidelines for disabilities, add, drop, appeals, etc. Notice that we have zero tolerance for cheating; as a result, please read the Policy Statement on Academic Misconduct carefully. Also, you should be aware of the SIC Policies and Guidelines.

Class rosters are provided to the instructor with the student's legal name as well as 'Preferred first name' (if previously entered by you). In the Student Profile section of your SIS account. While CS refers to this as merely a preference, I will honor you by referring to you with the name and pronoun that feels best for you in class, on papers, exams, group projects, etc. Please advise me of any name or pronoun changes (and please update CS) so I can help create a learning environment in which you, your name, and your pronoun will be respected.

Grading
The following items will be considered for evaluating the performance of students.

<table>
<thead>
<tr>
<th>Item</th>
<th>Fraction</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework Assignments</td>
<td>30%</td>
<td>as scheduled below</td>
</tr>
<tr>
<td>Midterm Exam</td>
<td>30%</td>
<td>in-class, Thu., February 21st</td>
</tr>
<tr>
<td>Final Exam</td>
<td>40%</td>
<td>08:00AM - 10:00AM, Wed., April 23rd</td>
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</tbody>
</table>

Homework Assignments
Homework assignments will be released on Canvas; all submissions must be made through Canvas. Only those submissions made before midnight will be accepted. Any late submission will be considered as no submission.

<table>
<thead>
<tr>
<th>Homework</th>
<th>Release Date</th>
<th>Submission Deadline</th>
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<tbody>
<tr>
<td>Homework 1</td>
<td>01/10</td>
<td>01/17</td>
</tr>
<tr>
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<td>01/17</td>
<td>01/24</td>
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<tr>
<td>Homework 3</td>
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<tr>
<td>Homework 4</td>
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<td>Homework 5</td>
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<tr>
<td>Homework 9</td>
<td>04/11</td>
<td>04/18</td>
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Class Schedule (subject to change)
The following is a tentative class schedule. Updated lecture slides will be posted on the morning before the lecture.

<table>
<thead>
<tr>
<th>Date</th>
<th>Lecture Topic</th>
<th>Slides/Video</th>
<th>Required Reading</th>
<th>Assignment Release</th>
</tr>
</thead>
</table>
Teaching Assistants

- Sumanth Gudaparthi
  - Email: sgudapar@cs.utah.edu

- Lin Jia
  - Email: lin.jia@utah.edu

- Jac MacHardy
  - Email: macharjk@gmail.com

- Taylor Smith
  - Email: taysmith16@gmail.com
Resources and Requirements


- Pre-requisite: Knowledge of structured programming languages such as C/Java
Course Expectation

- We use Canvas for homework submissions, grades, and homework announcements.

- Grading

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<td>Monday, April 29th</td>
</tr>
<tr>
<td>Class Participation</td>
<td>--%</td>
<td>Questions and answers in class</td>
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- Only those submissions made before midnight will be accepted.
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- You may skip 1 out of 10 (= we drop one HW with the least score).

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Academic Integrity

- Do NOT cheat!!
  - Please read the Policy Statement on Academic Misconduct, carefully.
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  - For more information, please refer to the important policies on the class webpage.
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- Understand what is inside a computer systems?
- Want to use the knowledge from this course in your own field of study?
- Understand the technology trends and recent developments for future computing?
- …
Why study computer organization?

- Do the conventional computers last forever?
  - New challenges
  - New forms of computing
Why study hardware?

- Better understanding of today’s computing problems
  - Security flaw: Spectre and Meltdown
Why study hardware?

- Better understanding of today’s computing problems
  - Security flaw: Spectre and Meltdown

- How to fix?
Estimated Class Schedule

- Moore's Law, power wall, bandwidth wall
- Use of abstractions
- Assembly language
- Computer arithmetic
- Pipelining
- Using predictions
- Memory hierarchies
- Reliability and Security
Growth in Processor Performance
Growth in Processor Performance

- Main sources of the performance improvement
  - Enhanced underlying technology (semiconductor)
    - Faster and smaller transistors (Moore’s Law)
  - Improvements in computer organization/architecture
    - How to better utilize the additional resources to gain more power savings, functionalities, and processing speed.
Moore’s Law

- Moore’s Law (1965)
  - Transistor count doubles every year

- Moore’s Law (1975)
  - Transistor count doubles every two years

Source: G.E. Moore, ”Cramming more components onto integrated circuits,” 1965
What are New Challenges?

- Resources (transistors) on a processor chip?
- Can we use all of the transistors?
- Who is affected?
What are New Challenges?

- Resources (transistors) on a processor chip?
  - Not really, billions of transistors on a single chip.
- Can we use all of the transistors?
  - Due to energy-efficiency limitations, only a fraction of the transistor can be turned on at the same time!
- Who is affected?
  - Server computers by the peak power
  - Mobile and wearables due to energy-efficiency
Power Consumption Trends

\[ \text{Power} = P_{\text{dynamic}} + P_{\text{static}} \]

\[ P_{\text{dynamic}} = axCxV^2xf \]

\[ P_{\text{static}} = VxI_{\text{static}} \]

Source: Hennesy & Patterson Textbook
What are New Challenges?

- Bandwidth optimization becomes a primary goal for memory design (*Bandwidth Wall!*)
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- Bandwidth optimization becomes a primary goal for memory design (Bandwidth Wall!)

Interconnect Bandwidth is Falling Behind at a comparable rate

- Peak FLOPS per Idle Memory Latency
- Peak FLOPS / Word of Sustained Memory BW
- Peak FLOPS / Word of Sustained Network BW

RISC systems (IBM, MIPS, Alpha) vs. x86-64 systems (AMD & Intel)


- +24.5%/year
  - 2x / 3.2 years
- +22.3%/year
  - 2x / 3.4 years
- +14.2%/year
  - 2x / 5.2 years
What are New Challenges?

- Can in-package memory solve the problem?

Off-chip Memory
- Lower Bandwidth
- Lower Costs

3D Stacked Memory
- Higher Bandwidth
- Higher Costs
What are New Challenges?

- Protecting data against side channel attacks is a serious need
- Performance in the past 40 years increased
  - hardware speculation to exploit more instruction level parallelism
  - shared memories to facilitate thread-level parallelism
- What about security?
  - https://meltdownattack.com/
Unconventional Computing Systems

- How to program a Quantum computer?
  - Qbit vs. bit
Emerging Non-volatile Memories

- Use resistive states to represent info.
  - Can we build non-von Neumann machines?
    - In-Memory and In-situ computers
Next Class

- Lecture: Measuring Performance
- Todo: order the textbook