

Novel Design Methodology for High-Performance XOR-XNOR Circuit Design

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Abstract

As we scale down to deep submicron (DSM) technology, noise is becoming a metric of equal importance as power, speed, and area. Smaller feature sizes, low voltage, and high frequency are some of the characteristics for DSM circuits. A novel design methodology for the design of energy-efficient noise-tolerant XOR-XNOR circuits that can operate at low voltages is proposed. The proposed circuits are characterized and compared with previously published circuits for reliability and energy efficiency. To test their driving capability, the proposed gates are implanted in an existing 5-2 compressor design and is shown to provide superior performance. The average noise threshold energy is used for quantifying the noise immunity. Simulation results show that the proposed circuits are more noise-immune and displays better power consumption results as well as power-delay product characteristics. Also, the circuit s prove to be faster and successfully works at all ranges of supply voltage starting from 0.6V to 3.3V.

Keywords - Design methodology, Noise-tolerance, low power, XOR-XNOR.

1. Introduction

The XOR and XNOR gates play the major role in various circuits especially circuits used for performing arithmetic operations like full adders, compressors, comparators, and so on [1]. Optimized designs for XOR and XNOR gates are needed to benefit the performance of larger circuits that they are part of. What is meant by optimized design is to avoid any degradation on the output voltage, consume less power, having less delay, and be noise immune even with low voltage as in deep submicron technology. Another desired feature for the design of a combined XOR-XNOR cell is to have a small number of transistors to implement it [2] and the simultaneous generation of the two non-skewed outputs.

Several designs were proposed to realize the XOR function using different logic styles [3]. Two optimized designs are shown in Fig. 1. The first design is based on utilizing the high functionality of pass-transistor logic style [4]. This circuit has a non-full voltage swing at the output node and is characterized by its low power consumption. This circuit has a limited driving capability. The second circuit is using static CMOS inverter in conjunction with a MUX circuit. The availability of the inverter gives signal level restoration and improves the driving capability of the circuit but these come at the expense of extra power consumption.

In large designs, multipliers have been a critical component dictating the overall circuit performance. In fast multipliers, partial products accumulation is implemented using a summation tree, called the Carry Save Adder (CSA) tree. Designs for CSA tree uses either full adders or compressors like the (4-2) compressors for interconnect regularity. High input compressors such as (5-2) and (6-2) have also been studied and reported in the literature. The XOR-XNOR and multiplexer functions represent the core of the compressor cell according to the nature of the logic operation. The combined XOR-XNOR cell is used to drive the selection lines of the multiplexer. The generation of XOR and XNOR simultaneously proves to be vital for this purpose. The two control signals, select and select bar, are required to reach the multiplexer simultaneously to avoid glitches and decrease the power consumed by these glitches.

Another design for XOR and XNOR gates using 4-transistors each was presented in [5] (see Fig. 1b). These were called the power-less and ground-less (P-/G-) circuits respectively. These circuits proved to be power-efficient but they displayed poor delay characteristics. All these designs are plagued by the basic disadvantage of pass transistors i.e. bad output levels. Also, these designs are unable to function properly when the supply voltage is scaled down as in nanometer technology. A 10-transistor design for producing XOR and its inverted output is shown in Fig. 2. This circuit rectifies the flaws in the previous designs. The design is composed of two transmission gates

and three static inverters. The circuit provides good output levels for all combination of inputs due to the functionality of the transmission-gate making it suitable of working at lower supply voltages. The driving capability of the circuit is also improved as it uses static inverters. The main disadvantage of the circuit is its power consumption due to the presence of the three static inverters. Also, the two output signals are heavily skewed in time.

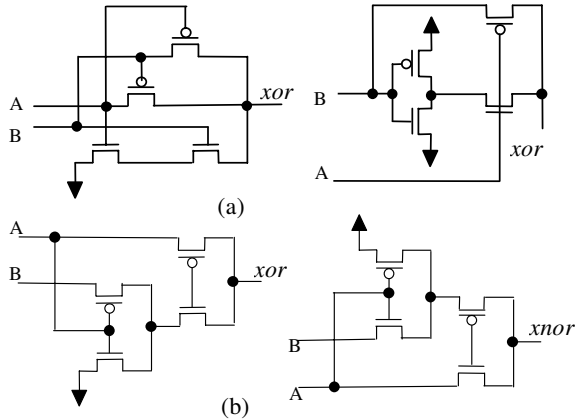


Figure 1. (a) Optimized implementations for XOR function. (b) Power-less XOR and Ground-less XNOR.

To overcome the problem of skewed outputs an efficient design that combines the implementation of both the XOR and the XNOR functions in one circuit using only 6 transistors is presented in [2] (see Fig. 3a). The circuit has a single connection to Vdd and a single connection to Gnd with no direct connection between them. The existence of Vdd and Gnd connections give good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component. An improved version of this circuit [6] (see Fig. 3b) has a better power-delay product and higher noise-immunity.

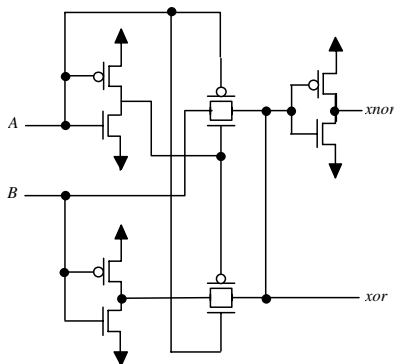


Figure 2. 10 transistor circuit for XOR-XNOR function.

In this paper, an attempt has been made to generalize a methodology for building low-power high-speed XOR-XNOR circuits for arithmetic circuits.

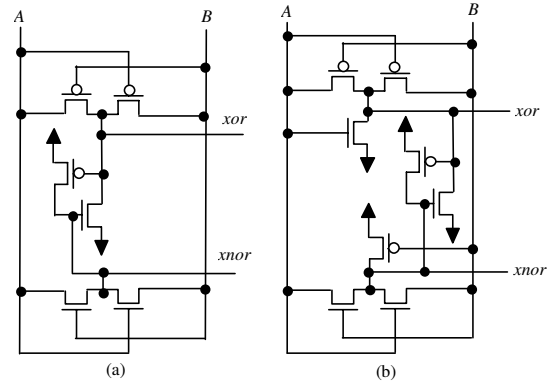


Figure 3. XOR-XNOR circuit by [2] and [6].

2. Proposed Methodology

As mentioned earlier, each of the design units in Fig. 1 produces bad logic levels at the output. These circuits may work at higher supply voltages but at lower voltages, this behavior is intolerable. As we scale down the supply voltage, a reliable design is required to provide high performance in noisy environment. An example of the output for P-/G- designs is shown in Fig. 4. Consider the XOR-gate in Fig. 1a. The circuit produces bad logic levels when input 'B' is low. The corresponding XNOR-gate will produce bad outputs in the exactly opposite input cases i.e. when input 'B' is high. Now, consider Fig. 1b. In XOR-gate, output is at bad level when input 'A' is low and in XNOR-gate, when input 'A' is high. To rectify this behavior, we propose a novel design methodology. By adding transistors to the design and combining the XOR and XNOR-gates, we obtain a new circuit that exhibits better performance.

The first solution is to add a feedback between the XOR and XNOR-gate and use additional transistors to rectify the levels at specific inputs (see Fig. 5a). It was observed that if the source inputs to the XNOR gate are switched and the gate input of both transistors is made \bar{A} , then the resulting circuit is faster. This is owing to the fact that PMOS transistor is inherently slow and an inverted signal was passed through a PMOS transistor adding to the delay.

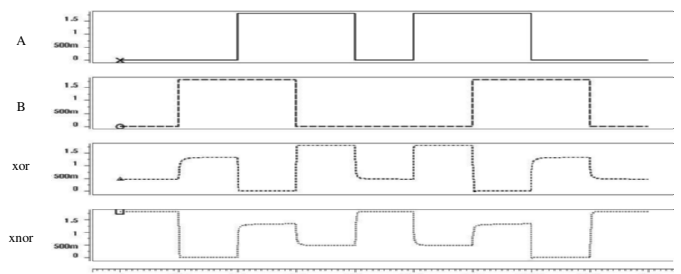


Figure 4. Output for P-/G- designs at 1.8v at 0.18μ technology.

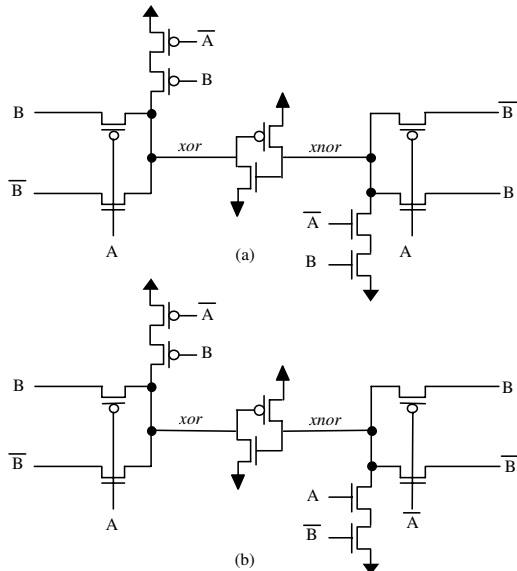


Figure 5. Proposed methodology with single feedback and add-on transistors.

The second solution is to add dual feedbacks. The resulting circuits are shown in Fig. 6. Note that the case when we switch or reverse the inputs still applies to this methodology also. We tested out methodology on standard designs for example the P-/G- XOR-XNOR gates. After application of the methodology, the output levels of the gates became good for all input combinations and made the circuit suitable for operation in low voltages. There is a trade off between the two proposed methodologies i.e. the first one improves speed of operation to a greater extent while the second enhances the power-consumption statistics greatly. The proposed designs prove to be noise tolerant and provide a significant improvement in the power-delay product in each case. These are investigated in the following sections.

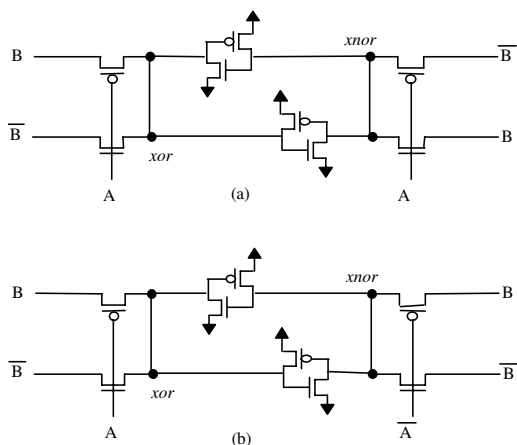


Figure 6. Proposed methodology with dual feedback.

3. Noise Metrics

In this paper, we use the noise immunity curves, NIC, [7] to measure the noise-tolerance of XOR-XNOR circuits. The noise immunity curve of a digital gate is a locus of points (T_n, V_{DD_n}) for which the gate just makes a logic error. All noise pulses below the NIC do not cause any errors. Hence, the higher the NIC of a gate, the less susceptible is the gate to noise. For a quantitative value of noise immunity, a metric called *average noise threshold energy* (ANTE) is derived from the noise immunity curve. It is a measure that can be employed to compare the noise signature of various gates. This metric is given by:

$$ANTE = E(V_{noise}^2 T_{noise})$$

where $E(\)$ denotes the expectation operator. These noise metrics is widely implemented [8][9]. For simulation purposes, we generate a noise pulse using a noise injection circuit as shown in Fig. 7 [10]. The circuit basically is a tunable delay line to provide a noise pulse of the desired width and amplitude so as to produce a glitch in the output.

4. Simulation Results

In this section, the performance of the proposed methodologies is investigated. Noise-tolerance and circuit performance of the proposed XOR-XNOR designs are compared with previously existing circuits shown in Fig. 2 ('previous' in figures). The reason that we chose this circuit for comparison is as that it can operate at low supply voltages and has a good output level. We also compare the results with circuit in Fig. 3b. We simulate both the versions of the circuits given in Fig 5 and 6 and name them proposed circuit 1 and 2. Each of the two versions is called 'with reverse inputs' and 'without reverse inputs' respectively in the simulation result figures.

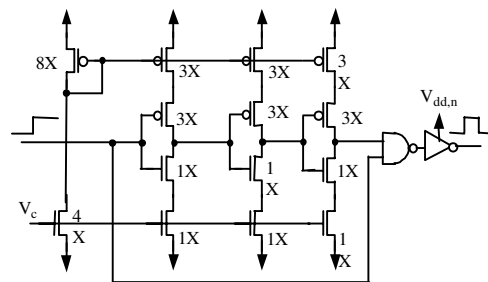


Figure 7. The Noise Injection Circuit.

The resulting noise immunity curves are shown in Fig. 8. This figure shows that the NICs for the proposed XOR-XNOR circuits are much higher than the compared one showing that it has higher noise-immunity. The ANTE for the proposed circuit 1 is 2.16 (XOR) and 1.78 (XNOR) times better than the existing circuit under comparison (see Table 1).

Table 1. ANTE results.

ANTE Value	Previous	Proposed 1
XOR	0.3017	0.6490
XNOR	0.4410	0.7825

The circuit performance of the XOR-XNOR circuits is evaluated in terms of worst-case delay, power consumption and power-delay product for all ranges of supply voltages (0.6v to 3.3v). The results are shown in Fig. 9. These figures show that the proposed XOR-XNOR circuit 1 with reverse inputs is faster than the previous one but a little slower than the circuit in [6]. The proposed circuit 1 consumes less power and the power delay product is much better than the previous one as well as the circuit in [6]. Proposed circuit 2 also shows similar results in terms of power-consumption and power-delay product but in terms of speed of operation, it lags behind proposed circuit 1.

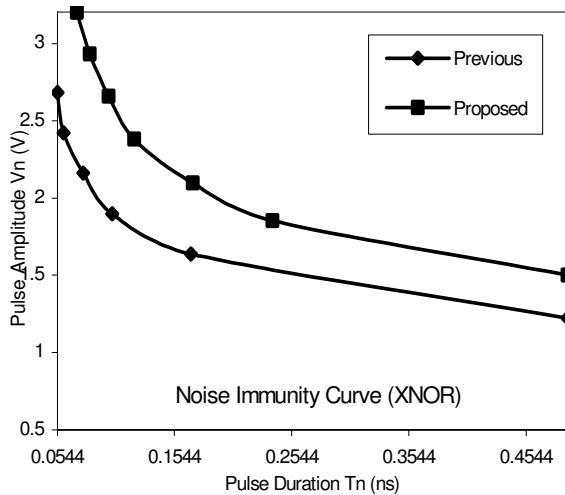
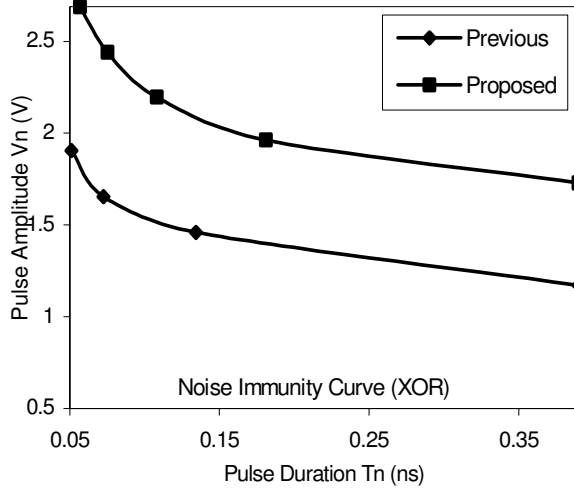
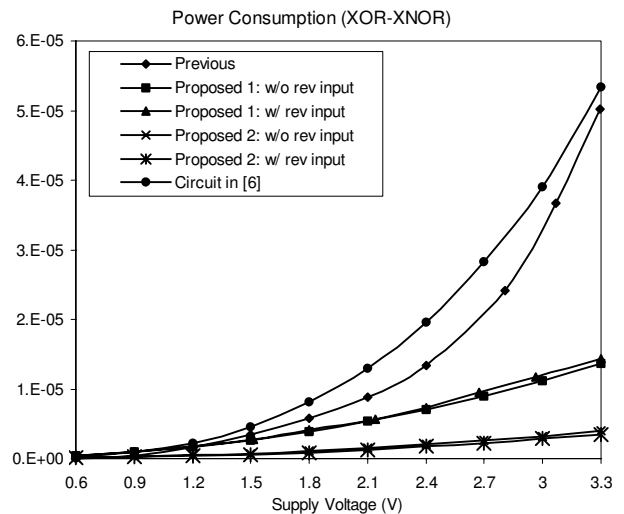
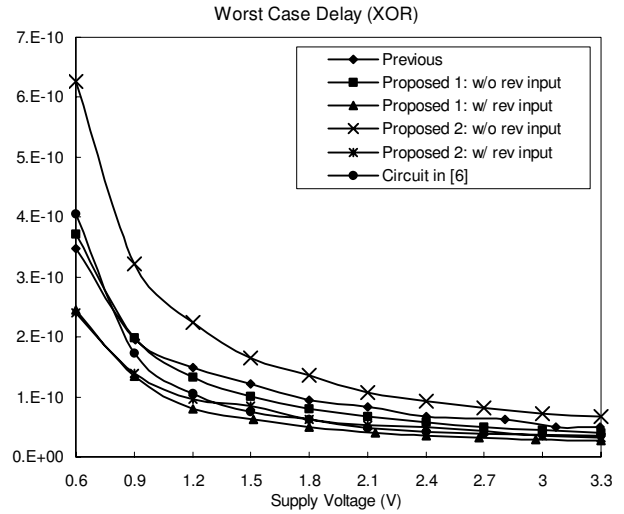
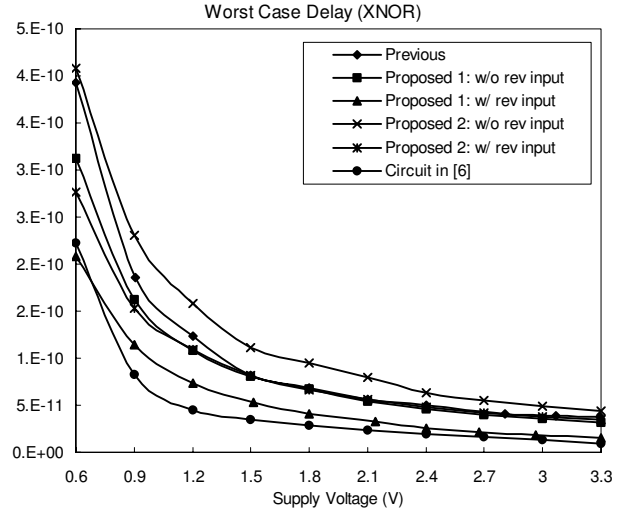


Figure 8. Noise immunity curves for the proposed XOR-XNOR and the compared one.



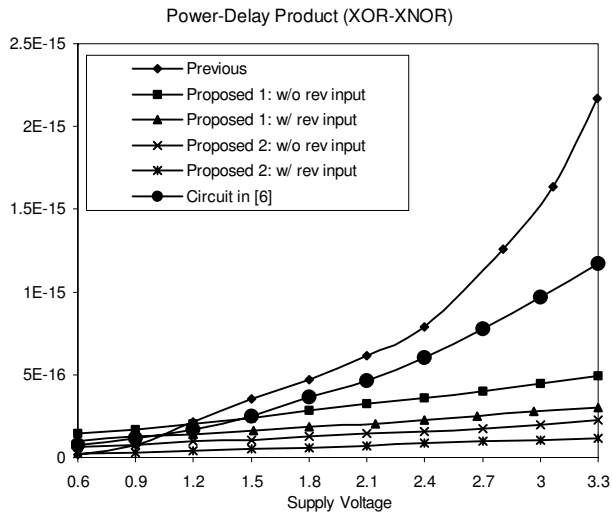


Figure 9. Simulation results for XOR-XNOR circuits.

The important observation to be made here is that the proposed circuit with reverse inputs proves to be better than the circuit without reverse inputs in each case.

Also, a 5-2 compressor circuit, Fig. 10 from [10], is built with the studied XOR-XNOR circuits. This is done to compare the circuits comprehensively in a real application. The multiplexer used for the 5-2 compressor is shown in Fig. 11. This multiplexer is widely used for carry output generation in fast full adders and multi-input compressors [2]. A buffer is added to enhance the driving capability. Buffered inputs are provided to the compressor for realistic simulation conditions. 1024 input combinations resulting from 7 inputs are used to obtain an average power consumption statistic for the compressor. Worst-case delay and power consumption is calculated at 1.8v V_{dd} . The results are shown in Table 2.

It is clear that the architecture with the proposed circuit occupies approximately the same area but it consumes slightly less power. Also, the power delay product for the architecture with the proposed circuit is better than the compared one. In addition to these results, that architecture is much noise-immune as shown previously.

Table 2. Simulation results for 5 to 2 compressor.

	Previous	Proposed
Power Consumption (μ W)	57.42	54.11
Worst-Case Delay (ns)	0.081	0.044
Power-Delay Product	4.65102	2.38084

5. Conclusion

We have proposed and tested a novel design methodology for noise-immune low voltage XOR-XNOR circuits. The performance of the proposed circuits has been shown to outperform the compared ones, which can operate

at low-voltages, and have good output levels. The proposed circuits have been tested to be much noise-immune, energy-efficient and faster than the compared ones. The ANTE for the proposed circuit 1 is 2.16 (XOR) and 1.78 (XNOR) times better than the existing circuit under comparison. Also, the circuits have been tested inside a real environment. We picked the 5-2 compressor architecture to test the circuit inside it, as it is a critical component in any fast multiplier architecture. The power delay product for the architecture with the proposed circuit has been shown to outperform the one for the same architecture with the already existing XOR-XNOR. As a future work, we plan to measure the effect of including this circuit in a real system and see how much noise does it generate and affect the power supply.

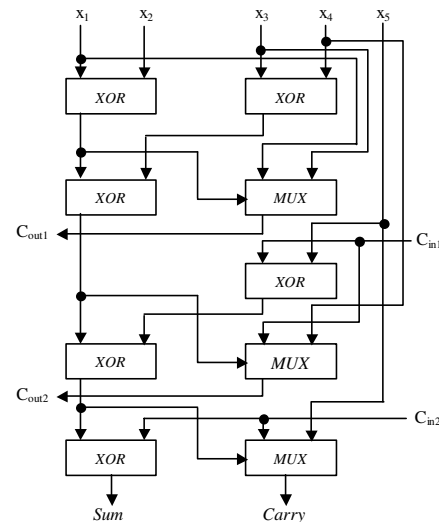


Figure 10. 5-2 Compressor architecture.

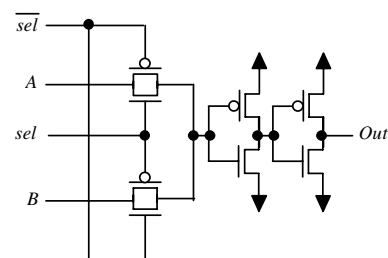


Figure 11. 2 to 1 Multiplexer cell.

6. Acknowledgments

The authors acknowledge the support of the U.S. Department of Energy (DoE), EETAPP program, DE97ER12220 and the Governor's Information Technology Initiative.

7. References

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