

Low Power MIPS Processor Design

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Abstract — Power consumption has become one of the major challenges in IC design. The paper presents two power-saving methods applied to MIPS processor design: clock gating and multi-voltage power supply. The experiments showed that clock gating scheme saved more than 65% power of baseline implementation while decreased performance by 45%. Also we have successfully implemented a multi-voltage designed MIPS processor even though we face several problems along the way.

Index Terms — VLSI, multi-voltage supply, MIPS, critical path

I Introduction

Our prime objective is to implement a power-efficient MIPS microprocessor. This objective was motivated by the fact that nowadays IC designs have become more complex; reducing power consumption has become the first factor to be considered for IC design. Especially, this demand is increasing for battery-based electronic systems, like laptops, cellular phones and so on.

There are three well-known power-saving optimization methods as far as we know: clock gating, back body biasing and multi-voltage supplies (MSV) are those methods. We first researched back body biasing, however we found out that there are only a limited number of documents available, we chose clock gating and MSV as our power-saving methods to decrease the power consumption.

We implemented clock gating first and then applied MSV to our baseline MIPS implementation. Specifically, we implemented clock gating to the baseline implementation and made a detailed comparison analysis about performance and power. The result shows that clock gated MIPS saves 65% of power comparing to the baseline. There is some reduction on performance. However, we found out that the power delay product is much better on clock-gated MIPS processor.

The concept of MSV is to segregate the power for specific modules and reduce voltage of some modules that do not lie on the critical path while retaining the performance of the whole chip unchanged. The critical problem here is to determine the critical module region from non-critical modules. One of the solutions we found was to get the critical path using PrimeTime-PX and then analyze the critical path which helped us to obtain the critical modules. Moreover, we found out that dividing the modules into several sub-modules increased the non-critical area. Our project has implemented a baseline MIPS (8-bit) microprocessor and a clock gated version of the baseline. Based on the two versions of MIPS, a detailed analysis was made. Also, we implemented MSV applied MIPS processor with LVS-bypassing scheme.

II Project Design

2.1 Multi-Voltage CMOS Designing

The key idea of the MSV project design is that we divide the whole MIPS processor into different modules based on the functional similarity. By doing this, different parts are functionally independent. However, from the whole chip prospective view, they are connected to each other.

At the very beginning, flattened MIPS processor is built. It is a baseline for our design and all other design should be compared with the baseline. And then MIPS processor is divided into three parts, which are *datapath*, *controller* and *alucontroller*. Those three modules are used for building the unflattened MIPS processor. We figure out delay for each module. Based on the delay information, we can determine the critical path for the entire chip. The relationship between the voltage supply and the delay is that the higher the voltage supply, the smaller the delay. So we can determine the voltage supply for each module based on the delay, of which the critical path is connected with the highest voltage supply.

Voltage Shifter (Voltage Interface Circuit) is another important module for the design. Due to the different voltage supplies for different modules, a potential problem arises: when the output of the low voltage supply is used for driving the high voltage domain, it is possible to fail. To solve the problem, we have to introduce a voltage shifter. We provide two different kinds of voltage

We define critical paths by its latency. If the latency of the specific path is the largest one, then it is the critical path in the circuit and other paths are non-critical paths, which are shown in figure 3.

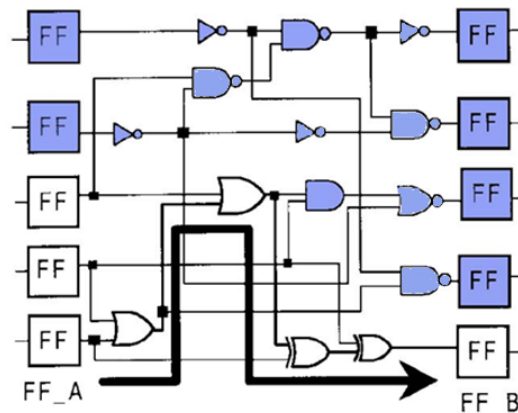


Figure 3: critical path and non-critical path based on latency. The dark line shows the critical path of this circuit. The blue cells are on the non-critical paths.

2.2 Clock Gating Designing

Clock gating is one of the power-saving techniques used on many synchronous circuits. To save power, clock gating support adds additional logic to a circuit to prune the clock tree, thus disabling portions of the circuitry so that its flip-flops do not change state: their switching power consumption goes to zero, and only leakage currents are incurred. Figure 4 shows a simple clock gated register. Since there is only one register, the block is 100% clock gated.

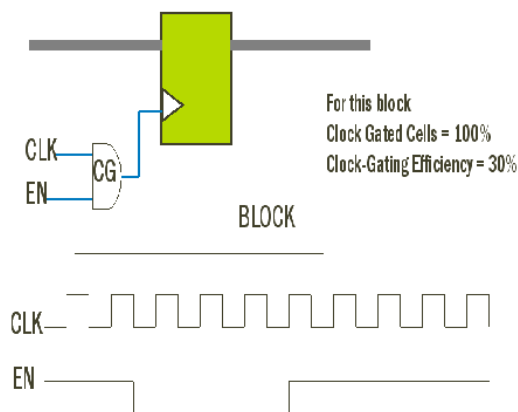


Figure 4: clock gating

III. Design Implementation

3.1 General Design Process

The design approach for this project, in terms of actual chip design, is centered on independent module operations; that is, the various modules that make up the entire chip should be able to be implemented without depending on other modules. This approach allows different parts of a chip to be designed in parallel, and therefore speeds up the process of implementing chips.

Here is our design flow:

1. Simulation to verify the functionalities.

Since the source code of MIPS is available, so at the very beginning, we should verify the functionalities of MIPS to make sure it is right.

2. Synthesis

After confirming the functionality, the next step is to finish synthesis. When doing synthesis, we tried different clock periods to get the best one which makes the slack time minimized. After synthesis, we can get .rep file and .pow file which contain timing, area, and power information.

3. Timing and Power Analysis

Here from the timing report file, we can also determine the critical path which can be used to determine the modules which are not in the critical path and therefore to reduce the voltage on those modules.

4. Floorplaning, Routing & Placement

5. Timing and Power Analysis

In order to get the accurate version of timing and power information, we should files generated by Soc-Encounter, .sdf(stand delay file) and .spef files which contain parasitic components of circuit, gate information and RC parasitic information.

6. Padding

After the placement and routing, we have to import files into cadence to get the Corresponding schematic and layout view of the design. After verifying that every module is available now, we use CCar to synthesize them together to get the chip.

Another important thing is that we need to put the core of the chip into the pad ring. By changing the schematic and layout view of the pad ring, we make sure that it can be used for our core.

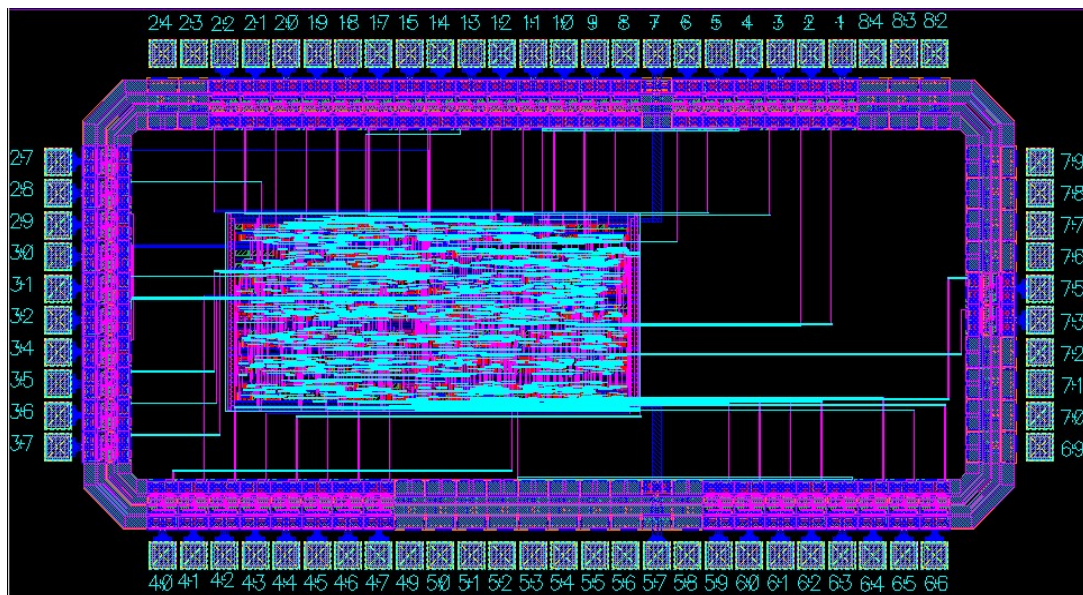


Figure 5: The final clock-gated MIPS

3.2 MSV Implementation

On implementation of multi-voltage MIPS design, we faced several challenges on the way... The first one was the problem of labored insertion of voltage interface circuits. The second one was passing LVS on the chip.

The first problem was solved by manually adding voltage interface cells to the *struct.v file.

3.3.1 Modifying *struct.v for manual voltage interface insertion.

For example, if we have a datapath_struct.v file on this format.

```
module datapath ( clk, ... );  
  input clk, ...;
```

```

...
DFFX1 ir0_q_reg_0_ ( .D(n512), .G(clk), .CLR(n273), .Q(instr[0]) );

```

We had to manually change the datapath_struct.v file like this.

```

module datapath ( clk, ... );input clk, ...;
wire clkP;

```

```

...
INTERFV3X6 U100( .A(clk), .Y(clkP) );
DFFX1 ir0_q_reg_0_ ( .D(n512), .G(clkP), .CLR(n273), .Q(instr[0]) );

```

(Note: The index of the new cells must be maintained. If the previous maximum cell index number was 99, the added new cell's index begins from 100.)

From this manner, we were able to make a chip that supports low voltage input drive. The final layout of the multi-voltage supply MIPS is shown as figure 6.

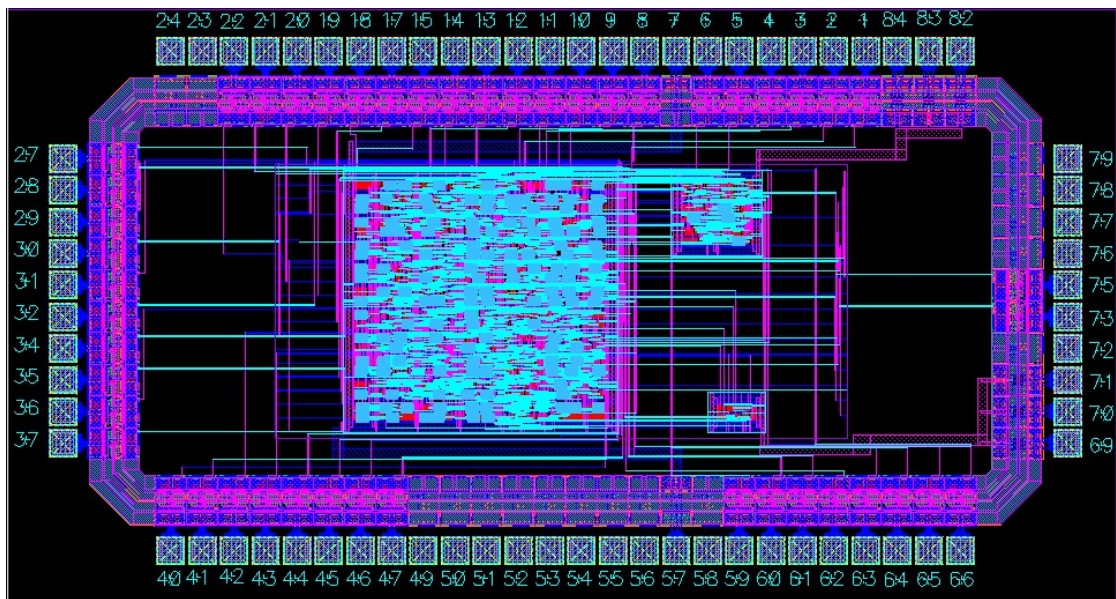
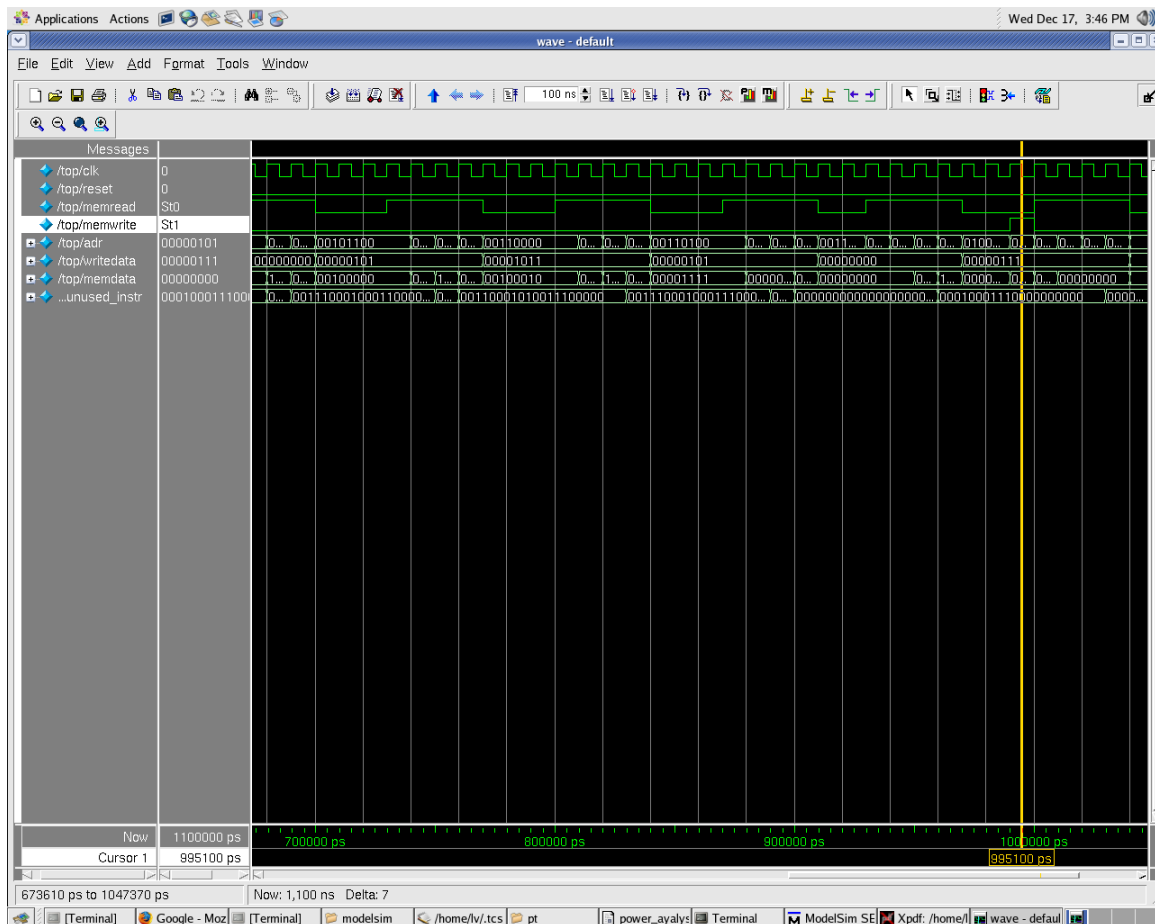


Figure 6: the final layout of Multi-voltage supply MIPS. The voltage interfaces are integrated into the datapath. For more detail, please refer to the section 3.3.1.

IV Experiments and Analysis

1 Simulation

Before making further move, we should first make the functionalities of MIPS are right.



2 Timing analysis

We have timing reports from both Design Compiler and PrimeTime-PX and we present both them here, so we can eye the timing information in different views. Also we make a comparison between MIPS based on our library (Lib6710_02) and library from UofU_Digital_v1_2.

2.1 Timing of Lib6710_02

First, timing information from Lib6710_02-based MIPS is showed in Table I and Table II.

Table I delay of LIB6710 from DC

<i>datapath</i>	<i>alucontrol</i>	<i>controller</i>	<i>critical path</i>
13	3	6	19

Table II delay of LIB6710 from PT

<i>datapath</i>	<i>alucontrol</i>	<i>controller</i>	<i>critical path</i>
14	3	7	21

Because Lib6710_02 is used to generate MIPS based on modules, we first obtain each module's delay information and then only add up the delays that are on critical path. Table I shows the delay of LIB6710 from DC. Table II shows the delay of LIB6710 from PT. Timing from PT is greater than that of DC.

2.2 Timing of UofU_Digital_v1_2

Second, timing information from UofU_Digital_v1_2-based MIPS is showed in Table III and Table IV.

Table III delay of UofU_Digital_v1_2 from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>
timing	19	33
rate	1	1.74

Table IV delay of UofU_Digital_v1_2 from PT

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>
timing	20	33
rate	1	1.65

Table III shows the baseline and clock gating delay from DC. Clock gating delay is about 74% more than baseline delay. The reason is that clock is inserted in any possible flip-flop circuits. As a result, the delay is increased. Table IV shows the baseline and clock gating delay from PT. It is the same reason why clock gating delay is about 65% more than baseline delay.

2.3 Timing Comparison and results

Third, we make a comparison among all the delays, illustrated by Table V and Table VI.

Table V delay comparison from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>	<i>baseline-LIB6710</i>
timing	19	33	20
rate	1	1.74	1.05

Table VI delay comparison from PT

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>	<i>baseline-LIB6710</i>
timing	19	33	21
rate	1	1.74	1.11

The result shows that baseline version of MIPS from UofU_Digital_v1_2 library is much better than clock gating version from UofU_Digital_v1_2 library and baseline version from Lib6710_02.

3 Power Analysis

We also have power reports from both DC and PT. Meanwhile, we make a comparison between MIPS based on our library (Lib6710_02) and library from UofU_Digital_v1_2.

3.1 power of Lib6710_02

Table VII power information of Lib6710_02 from DC

	<i>Cell Internal</i>	<i>Net Switching</i>	<i>Cell Leakage</i>	<i>total</i>
<i>datapath</i>	40.8318 mW	5.9885 mW	97.5118 nW	46.8203mW
<i>alucontrol</i>	1.7168 mW	595.7427 uW	883.3262 pW	2.3125mW
<i>controller</i>	4.2593 mW	1.1026 mW	6.3379 nW	5.3619mW

	<i>Cell Internal</i>	<i>Net Switching</i>	<i>Cell Leakage</i>	<i>total</i>
<i>total</i>	42.5486mW	6.5842mW	104.7330nW	54.4947mW

Table VIII power information of Lib6710_02 from PT

	<i>Cell Internal</i>	<i>Net Switching</i>	<i>Cell Leakage</i>	<i>total</i>
<i>datapath</i>	30.8mW	26.8mW	107.9nW	57.6mW
<i>alucontrol</i>	0.3776mW	0.2014mW	0.9509nW	0.5791mW
<i>controller</i>	4.003mW	3.212mW	7.960nW	7.215mW
<i>total</i>	35.1559mW	30.2134mW	116.8109nW	65.3694mW

Since the same reason, we first obtain each module's power information and then add up the all the powers of each module.

3.2 power of UofU_Digital_v1_2

Table 9 power information of UofU_Digital_v1_2 from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>
Cell Internal	38.6831 mW	11.4030 mW
Net Switching	2.3641 mW	1.2758 mW
Cell Leakage	113.6330 nW	103.6765 nW
total	41.0473mW	12.6789mW
rate	1.0000	0.3089

Table 10 power information of UofU_Digital_v1_2 from PT

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>
Cell Internal	37.7mW	11.3mW
Net Switching	10.3mW	5.110mW
Cell Leakage	121.2nW	106.4nW
total	48.0000mW	16.4101mW
rate	1	0.3419

As the tables illustrated, for the same library, clock gating saves a large number of powers, at least 65% reduction is achieved.

3.4 Power Comparison and Results

Table 11 power comparison from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>	<i>baseline-LIB6710</i>
Cell Internal	38.6831 mW	11.4030 mW	42.5486mW
Net Switching	2.3641 mW	1.2758 mW	6.5842mW
Cell Leakage	113.6330 nW	103.6765 nW	104.7330nW
total	41.0473mW	12.6789mW	54.4947mW
rate	1.0000	0.3089	1.3276

Table 12 power comparison from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>	<i>baseline-LIB6710</i>
Cell Internal	37.7mW	11.3mW	35.1559mW
Net Switching	10.3mW	5.110mW	30.2134mW
Cell Leakage	121.2nW	106.4nW	116.8109nW
total	48.0000mW	16.4101mW	65.3694mW
rate	1	0.3419	1.3619

We make a comparison among all the powers, as Table 11 and Table 12 showed. The result shows that clock gating version consumes less power than the other two versions, at most four times reductions.

4 Area Report

4.1 Area of Lib6710_02

Table 13 area of Lib6710_02

	<i>Combinational</i>	<i>Noncombinational</i>	<i>Total</i>
<i>datapath</i>	143986	132192	276178
<i>alucontrol</i>	3175	0	3175
<i>controller</i>	17042	3888	20930
total	164203	136080	300283

Since the same reason, we first obtain each module's area information and then add up the all the areas of each module to get the total area.

4.2 Area of UofU_Digital_v1_2

Table 14 area of UofU_Digital_v1_2 from DC

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>
Combinational	3259	2441
Noncombinational	2520	2663
Total	5779	5104
rate	1	0.88

4.3 Area Comparison and Results

Table 14 area comparison

	<i>baseline-UofU</i>	<i>clock gating-UofU</i>	<i>baseline-LIB6710</i>
Combinational	3259	2441	164203
Noncombinational	2520	2663	136080
Total	5779	5104	300283
rate	1	0.88	51.96

Obviously, the clock gating version holds the least area. However, here the number only reflects the number of cells.

The only reason for the increased number of cells is that UofU_Digital_v1_2 library is better than Lib6710_02 library.

V Conclusion and Discussion

Our team has successfully built up four versions of MIPS.

IV. flattened baseline MIPS uP

V. clock-gated flattened MIPS uP

VI. modular baseline MIPS uP

VII. modular three voltage MIPS uP

We were able to make full analysis on comparison of clock-gated and baseline MIPS processor. However, comparison of three voltage MIPS processor with baseline was not possible because we could not figure out the way to get *.sdf file from the LVS-bypassed layout. (Please, read the LVS-bypassing scheme we elaborated on Implementation section).

5.1 Clock Gated MIPS Processor

According to our experiments, the power of MIPS has been dramatically reduced on clock-gated MIPS processor. Almost 65% of the baseline's power has been reduced on clock-gated MIPS processor.

However, there were trade-offs between the speed, power and area. From the clock-gated experiment, we got power and area reduction, however the performance went down. The performance reduction was about 42%. Therefore, the delay * power metric shows $(1.74 * 0.342) = 0.595$ which means that the clock-gated chip is about 68% efficient than the baseline considering same weights to power and performance.

5.2 Multi-Voltage MIPS Processor

From the multi-voltage supply prospective, although the performance of the chip remains the same, the area of the chip increases as a penalty of the reduction in power. In essence, we have to make a trade-off between area, power and performance so that it can meet our requirement.

There are several potential reasons responsible for the failure of the unflattened MIPS with multi-voltage supply. First, the VDD and GND are not in the symbols of the modules. So if we try to implement more than one VDD to layout of the chip, they are not reflected on the schematic of the chip. Therefore, the schematic and the layout of the chip are not going to match. Second, it is possible that cadence allow us to have only one voltage supply. If we want to supply the chip with multi voltages, we have to finish it during the process of SOC. Third, the pin type of the pad ring may affect the result. We have tried to set the pin type of VDD as "pad_io_nores", but it doesn't work.

5.3 Conclusion

Our project has implemented a baseline MIPS (8-bit) microprocessor and a clock gated version of the baseline. Based on the two version of MIPS, a detailed analysis was made. However, for MSV, which is quite a hard method to implement. We implemented MSV applied MIPS processor until the LVS step. Somehow our Cadence tool does not recognize multiple voltages correctly. This drawback is compensated by PrimeTime-PX which can generate static power and timing information for MSV. As a result, we conduct all the comparisons and make a detailed analysis for all comparisons.

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