On the Decidability of Shared Memory Consistency Verification

Ali Sezgin and Ganesh Gopalakrishnan
{sezgin, ganesh}@cs.utah.edu

UUCS-05-009

School of Computing
University of Utah
Salt Lake City, UT 84112 USA

May 5, 2005 (05-05-05)

Abstract

We view shared memories as structures which define relations over the set of programs and their executions. An implementation is modeled by a transducer, where the relation it realizes is its language. This approach allows us to cast shared memory verification as language inclusion. We show that a specification can be approximated by an infinite hierarchy of finite-state transducers, called the memory model machines. Also, checking whether an execution is generated by a sequentially consistent memory is approached through a constraint satisfaction formulation. It is proved that if a memory implementation generates a non-interleaved sequential and unambiguous execution, it necessarily generates one such execution of bounded size. Our paper summarizes the key results from the first author’s dissertation, and may help a practitioner understand with clarity what “sequential consistency checking is undecidable” means.

1Supported in part by NSF grant ITR-0219805 and SRC Contract 1031.001.