A DRAM Backend for The Impulse Memory System

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Abstract

The Impulse Adaptable Memory System exposes DRAM access patterns not seen in conventional memory systems. For instance, it can generate 32 DRAM accesses each of which requests a four-byte word in 32 cycles. Conventional DRAM backends are optimized for accesses that request full cache lines. They may not be able to handle smaller accesses effectively.

In this document, we describe and evaluate a DRAM backend that reduces the average DRAM access latency by exploiting the potential parallelism of DRAM accesses in the Impulse system. We design the DRAM backend by studying each of its important design options: DRAM organization, hot row policy, dynamic re-ordering of DRAM accesses, and interleaving of DRAM banks. The experimental results obtained from the execution-driven simulator Paint [10] show that, compared to a conventional DRAM backend, the proposed backend can reduce the average DRAM access latency by up to 98%, the average memory cycles by up to 90%, and the execution time by up to 80%.

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