

Ultrapformance Wireless Interconnect Nanonetworks for Heterogeneous Gigascale Multi-Processor SoCs

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Abstract—To bridge the widening gap between computation requirements and communication efficiency faced by gigascale heterogeneous multi-processor SoCs in the upcoming billion-transistor era, a new on-chip communication system, dubbed Wireless Network-on-Chip (WNoC), is proposed by using the recently developed RF interconnection. With the uniqueness of wireless interconnection, the WNoC design paradigm calls for effective solutions to overhaul the on-chip communication infrastructure of nanoscale MPSoCs. In this work, we study the feasibility and applicability of wireless interconnection for on-chip communication.

I. PROBLEM DEFINITION

With continued scaling of microelectronics, silicon technology will allow chip complexity of up to one billion of transistors running at $10GHz$ by the end of this decade. As a result, gigascale system-on-chip (SoC) devices may utilize several hundreds or even thousands of processors yielding a “sea of processor”. When moving into such billion-transistor era, ever increasing complexity, heterogeneity, performance and productivity requirements put a heavy burden on next generation multi-processor SoC (MPSoC) design. The performance of gigascale MPSoCs will be limited by the ability to efficiently interconnect heterogeneous IP cores to accommodate their communication requirements. The state-of-the-art shared-bus and point-to-point connections have been shown unable to supply nanoscale MPSoCs with both sufficient bandwidth and low latency under a stringent power consumption limitation [1]. A scalable communication infrastructure with predictable bandwidth and latency is essential to provide plug-n-play interconnection of heterogeneous IP cores. Recently, the concept of Network-on-Chip (NoC) [2], has been proposed as the communication platform for complex MPSoCs by borrowing models, techniques and tools from the computer network design. In an NoC-based SoC, the cores access the network via on-chip routers (or switch) that forward packetized data and control signals to destination along a multi-hop routing path. NoC features prominent characteristics, such as transmitting packets instead of words, supporting parallel transaction, and solving clock skew problem in large-scale MPSoCs.

In the meantime, the speed improvements of silicon and SiGe bipolar transistors and MOS transistors have made the implementation of integrated circuits operating at ultra-high frequency feasible. According to ITRS [3], the cut-off frequency target for nMOS transistors is $280GHz$ by 2009 or at the $50nm$ CMOS node. With such transistors, it should be possible to build RF circuits operating at $90GHz$. Accordingly, quarter wave antennas for use in silicon will be

only $240\mu m$ long [4]. Consequently, as CMOS and BiCMOS technologies improve, the cost of on-chip antenna and required circuits will decrease dramatically, providing greater freedom to use on-chip radio. As a result, the new radio frequency (RF)/microwave technology is investigated for future intra-/inter-chip communication. A few initial steps have been taken to develop RF interconnect technologies, such as free-space transmission [5], guided-wave transmission [6], Ultra Wide-band (UWB) [7], and direct near-field coupling [8]. Among them, the introduction of UWB brings in new opportunity for high-data rate, low-power and short-range communication. Given its ultra-short transmission range and the isolated communication environment, an extremely wide spectrum is available, leading to great potential of achieving supereminent data rate, ranging from $150Gbit/s$ to $1.5Tbit/s$. The most recently-reported intra-chip UWB interconnection implementation has achieved $1.16Gbps$ data rate for single channel at central frequency of $3.6GHz$ in $0.18\mu m$ CMOS technology [9], [10]. A Si-integrated meander type dipole antenna has been implemented for $1mm$ range data transmission at antenna length of $2.98mm$. Table I summaries the area and power overhead for the transmitter and receiver design at $0.18\mu m$.

TABLE I
UWB INTERCONNECT IMPLEMENTATION IN $0.18\mu m$ CMOS

Transmitter	Power	21.6 mW	Area	$0.1 mm^2$
Receiver	Power	40 mW	Area	$0.54 mm^2$
Modulation	on-off keying (OOK)			
Data rate	1.16 Gbps (single channel)			
GMP central frequency	3.6 GHz			
Supply voltage	1.8 V			
Antenna type	meander type dipole			
Antenna	Length	2.98 mm	Distance	1 mm
Wireless channel	additive white Gaussian noise (AWGN)			

Using the Radio-on-Chip (RoC) technology, the chip-based wireless radios can be employed to replace the wires for increasing accessibility, improving bandwidth utilization, and eliminating delay and cross-talk noise in conventional wired interconnects. This brings forth a revolutionary on-chip communication infrastructure based on UWB interconnection, which we name as *Wireless Network on Chip (WNoC)* in contrast to NoC. WNoC will provide higher flexibility, higher bandwidth, reconfigurable integration, and freed-up wiring. With the uniqueness of RoC, existing NoC technologies cannot be applied in WNoC directly, calling for effective solutions to overhaul the on-chip communication infrastructure of nanoscale MPSoCs. System architecture and design technology must adapt to the critical challenges posed by both large scale integration and small device geometries.

II. WNoC SYSTEM ARCHITECTURE DESIGN

Based on the UWB interconnect technology, we propose to establish the WNoC for the communication among highly integrated heterogeneous IP cores with diverse functionalities, sizes and communication requirements in the gigascale MP-SoC. A WNoC architecture consists of two major components, i.e., *Transparent Network Interface (TNI)* and *Radio Frequency (RF) Infrastructure*. TNI serves as the interface between the IP cores and the WNoC. It diminishes the heterogeneity of the cores and interacts with the network fabric for packet assembly, delivery, and disassembly. We adopt a VCI-compliant TNI where the VCI embedded split protocol can ease the round-trip latency constraints between a request-response pair. A RF node hardware implements the WNoC data transmission protocol stack. The node is mainly equipped with routing decision logic, MAC unit, buffers and buffer management unit. Each node has a radio frequency interface (i.e., low-cost, low-power transceivers and tiny antennae) for (two-way) communication among IP cores. A number of RF nodes are dispersed on chip to form a multihop wireless nanonetwork. The IP cores access the network via TNI, and their packets are delivered to destinations through multiple hops across the network.

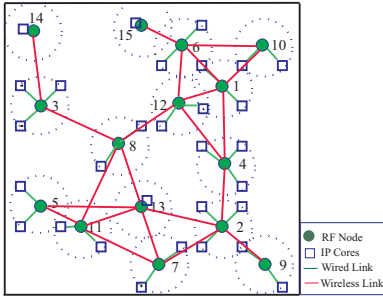


Fig. 1. Illustration of a WNoC topology formation.

In contrast to many NoCs that rely on regular topology, we propose a flexible RF network infrastructure tailored for gigascale MP-SoCs. To this end, we develop a self-configurable distributed multihop wireless nanonetwork architecture with custom irregular topology. The RF nodes are properly distributed chipwide according to various core functionality, non-uniform core size, and different traffic requirements between the cores. This flexible network architecture allows that several IP cores (small and/or low traffic) share one RF node or one IP core (big and complex with large I/O terminals) is associated with several RF nodes. The RF node communicates with each other through one or multiple “hops”. The IP cores might be grouped into clusters. Each core may have their own network interface or share network interface with other cores in the same cluster. The cores in a cluster are hard-wired to an RF node via network interfaces and share it for data/control communication. Given the short distance between IP cores and their associated RF node, the hard-wired connection results in minimum routing cost and area overhead. Formulation of RF node placement into disk covering, where a clustered wireless nanonetwork is abstracted as a set of disks, each centered at a RF node with a radius of R (i.e., the maximum RF node assistant distance) to cover a set of embedded IP cores

(wireless clients) on the chip plane, provides a high flexibility to construct a customized topology. Figure 1 illustrates a hypothetical WNoC topology with 15 RF nodes formed for an example MP-SoC of 30 IP cores.

III. WNoC PROTOCOL STACK DEVELOPMENT AND HARDWARE IMPLEMENTATION

Data transmission protocol is an integral part of the proposed on-chip wireless nanonetwork. Based on the WNoC architecture, we will design the data transmission protocol with the objective of making the implementation simple and efficient. Following the standard OSI layered structure, we propose to take a crosslayer design approach for developing transport, network and datalink layers. The *transport layer* adopts a simple approach similar to UDP (User Datagram Protocol) in the Internet, which leaves out complex flow control and error control by resource over-provisioning. Possible data loss is taken care in the application layer. In fact, the VCI protocol embedded in the VCI-compliant TNI already provides *Lossless data delivery* and *In-order data delivery* through the handshaking between the Requestor and Responder. Thus the transport layer is merely an interface between network independent layer (i.e., application layer) and network dependent layers (including all lower layers).

The major task of *network layer* is to determine the path from the source to the destination via single or multiple hops. The routing protocol must be customized for WNoC with its unique characteristics taken into consideration. *First, WNoC has extremely limited resources (e.g., circuit area and power) available on chip for the implementation of routing protocol. Second, it has fixed network topology with medium scale and density that is known prior to implementation. Third, it has very low delay tolerance for supporting the real time applications.* For cost-effective implementation of RF nodes, we develop a geographical distance routing scheme where the routing decision is made based on relative positions of the node and the destination node. The basic idea is that each node divides the entire chip area, from its own perspective, into several branches, with a particular neighbor as a branch header, and maintains a n -entry routing table (where n is the number of branches). Upon receiving a data packet, the node checks the destination’s location address contained in the packet header, and calculates in which branch the destination is located. Then, a proper next-hop node is chosen to forward the packet towards that branch. The routing decision tree based branch identification ensures minimum path cost and guarantees loop-free. The overhead involved in routing mainly stems from the implementation of routing logic (i.e., the location comparator) and the maintenance of routing information (e.g., the n -entry routing table).

As the nodes in WNoC communicate over the shared wireless medium, it is highly possible that two or more nearby RF nodes transmit data simultaneously which leads to collisions. The receiver in the collision region cannot receive the data packet correctly. Thus it is a key design issue to develop efficient *medium access control (MAC) protocol*

for resolving channel contention and minimizing collision probability, with two special requirements to be considered due to the uniqueness of WNoC. *First, the MAC protocol should have very low hardware implementation overhead, which prohibits the use of any conventional MAC protocols. Second, it should achieve very low collision probability and packet delivery delay, in order to meet the quality of service requirement of various on-chip applications.* We develop a dual-channel binary-countdown medium access control protocol, which involves a control channel and a data channel, such that the right to access the data channel is granted by the negotiation in the control channel. The MAC protocol is based on synchronized data frames, where each frame consists of two intervals: the contention interval and the data interval. The contention interval includes k contention slots and employs a binary countdown approach to resolve contention. A node (say, X) that has data to send generates a random number with k bits. If $b_i=1$, node X sends a one-bit contention signal, CS_i , in contention slot i . Otherwise, if $b_i=0$, X listens to the channel. If the channel is busy, X stops further transmission and gives up its attempt of gaining access to the channel in this frame. Such a synchronized and distributed MAC protocol ensures 100% collision free while having the features of high-efficiency, simplicity, robustness, fairness, and QoS capability.

Buffered flow control and buffer management are essential to improve WNoC end-to-end performance due to the close coupling between shared medium contention and network congestion. In order to avoid network congestion and improve end-to-end performance, it is necessary to control the traffic source to inject the packets into the network (especially for busy traffic) and manage the buffer communication along the traffic flows. We thus propose a distributed flow control and buffer management strategy involving multiple mechanisms: credit-based backpressure congestion control, fast forwarding by prioritized contention, virtual output queuing with a shared buffer, conditional round-robin output scheduling. The *backpressure congestion control* allows the upstream node on a node's flow to continue forwarding packets unless the previous upstream packet has been released to the downstream node. The *fast forwarding* grants higher priority for a downstream node (i.e., the node is a receiver in the last MAC contention) to increase its winning probability for the new-run of MAC contention. The *virtual output queuing with a shared buffer* maintains n output queues with one unit size each and a shared buffer with size of $n - 1$ units. This buffering scheme ensures dynamic allocation of upstream packets to a dedicated output queue corresponding to the dedicated downstream node. The *round-robin scheduling* triggers the next non-empty and non-blocking output queue for fair queue management.

Based on the proposed protocol stack, simple and compact RF nodes will be designed and implemented for establishing WNoC, that consists of three major components, namely, routing decision logic, MAC unit, and buffer management unit. In order to study the feasibility of WNoC for MPSoC applications, we estimate the power and area cost of a RF node using a power and area estimation tool called "InCyte Lite".

We further estimate the total power and area cost for a 10×10 QG WNoC for a MPSoC with 100 IPs on a $2 \times 2cm^2$ chip. It's feasible to assume that a NoC total area cost should be less than 5% of the total chip area. For a die size of $2 \times 2cm^2$, a 100-node NoC consumes about $20mm^2$ area or $0.2mm^2$ per network node. Table II lists the estimation of power and area cost of WNoC. We further look into the network throughput and end-to-end latency for 8×8 WNoC. In order to facilitate high bandwidth wireless data transmission, we acquire large packet size of 300 bits for $10Gbps$ data rate. Table III lists the throughput and latency at different traffic trace of WNoC.

TABLE II
AREA AND POWER ESTIMATION OF WNoC

Technology node	0.18 μm		0.13 μm	
	Power(mW)	Area(μm^2)	Power(mW)	Area(μm^2)
MAC Unit	1.8611	10890	0.8502	9050
RDL	0.5170	3024	0.2362	2514
BMU	2.7916	16330	1.2753	13576
Buffers	10.4962	189000	5.9040	37710
RF node	15.666	219400	8.2657	62850
10×10 QG WNoC	1.127 W	21.94 mm^2	595.13	6.28 mm^2

TABLE III
PERFORMANCE EVALUATION OF WNoC

Traffic (Trace injection divided by n)	$n=3$	$n=5$	$n=10$
Network Throughput (Gbps)	10.6	6.4	3.2
Avg. E2E Latency (cycles)	132.36	85.32	70.68
Max. E2E Latency (cycles)	1668	1212	1524

IV. SUMMARY

This paper centers on the design of WNoC from various crucial aspects such as physical characterization based on UWB interconnection, system architecture design, protocol stack development and hardware implementation. The heterogeneous nature of on-chip cores, and the energy efficiency requirements of high performance computing call for WNoC paradigm.

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