Chapter 7

Spectre Analog Simulator



Figure 7.1: The analog simulation environment for a circuit (DUT)

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| Hide | Cancel | Defaults | S | | He | |
| Library Cell View Names | NCSU_Analog_Parts Browse vdč symbol | | | | | |
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| AC magn AC phase DC volta | itude 9 ge | | <u>×</u> | | | |
| Noise file name | | | Ĭ | | | |
| Number of noise/freq pairs Temperature coefficient 1 | | | Q | | | |
| | | | Ľ | | | |
| Tempera | ure coerr | | | | | |
| Tempera Tempera | ture coeff | icient 2 | Į. | | | |

Figure 7.2: Component parameters for the vdc voltage source

| Edit | Object Properties | 1 | | | |
|---------------|---------------------|------------------------------|----------------|-------------|---------|
| ок | Cancel Apply | Defaults Prev | vious Next | | He |
| Apply Show | To only c | urrent - inst stem 🔳 user | tance | | |
| | Browse | Reset Ins | tance Labels E | Display | |
| | Property | | Value | | Display |
| | Library Name | NCSU_Anal | og_Parts | | off = |
| | Cell Name | vpulse | | | off 😑 |
| | View Name | symbol | | | off 🖃 |
| | Instance Name | VI | | | off 🖃 |
| | | Add | Delete | Modify | |
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| | lvsignore | TRUE | | | off 🖃 |
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| Voltag | e 1 | O V | | | off 🖃 |
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| Rise ti | ime | 1n s | ln š | | |
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| Pulse | width | 10n s | 10n s | | off 🖃 |
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| Tempe | erature coefficien | t 2 🛛 | | | off 🖃 |
| Nomin | al temperature | | | | off = |

Figure 7.3: Component parameters for the vpulse voltage source



Figure 7.4: Schematic for the nand-test DUT/testbench circuit

| Status: Ready | T=27 C Simulator: spectr | e |
|---|--|------|
| Session Setup Analyses | Variables Outputs Simulation Results Tools | Help |
| Design | Analyses | -Ę |
| Library test Cell nand2_test View schematic | * Type Arguments Enable | |
| Design Variables | Outputs | Γŧ |
| # Name Value | Name/Signal/Expr Value Plot Save March | |
| | Plotting mode: Beplace | • |

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Figure 7.5: Virtuoso Analog Environment control window

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| Analy | ysis | tran xf pz pac qpss qpsp | ✓ dc ✓ sens ✓ sp ✓ pnoise ✓ qpac | ◇ ac ◇ dcmatch ◇ envlp ◇ pxf ◇ qpnoise | ◇ noise ◇ stb ◇ pss ◇ psp ◇ qpxf | |
| | | Tr | ansient Anal | ysis | | |
| Stop Accu | Time racy Def conserva | 300r] aults (err ative r | preset) noderate | liberal | | |

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Figure 7.6: Choosing Analyses dialog box

| FileHelp6temp = 27 C tempeffects = all erpreset = moderate method = traponly lteratic = 3.5 relref = sigglobal cmin = 0 F gmin = 1 pS mos_wethod = s mos_wethod = s (26.4 %), step = 609.7 ps (203.8 %) tran: time = 127.9 ns (27.6 %), step = 609.4 ps (203.8 %) tran: time = 137.7 ns (52.6 %), step = 609.4 ps (203.8 %) tran: time = 137.9 ns (62.6 %), step = 609.4 ps (203.8 %) tran: time = 203.1 ns (62.6 %), step = 609.4 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 618.9 ps (206.6 %) tran: time = 222.8 ns (97.6 %), step = 609.2 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 609.4 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 618.9 ps (206.6 %) tran: time = 222.8 ns (97.6 %), step = 609.2 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 609.2 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 609.2 ps (203.8 %) tran: time = 222.8 ns (97.6 %), step = 609.2 ps (203.8 % | 💥 /uusoc/facility/res/async/elb/IC_CAD/cadence-f07/simulation 🛚 👁 🏊 🗔 💶 | IX |
|---|---|----|
| temp = 27 C tnom = 27 C trom = 105 matrixed = tromonly lteratic = 3.5 relref = sigglobal cmin = 0 F gmin = 1 pS maxred = 0 0hm mos_method = s mos_vres = 50 wV tran: time = 7.907 ns (2.64 %), step = 595 ps (196 m%) tran: time = 7.72 ns (12.6 %), step = 609.7 ps (203 m%) tran: time = 52.63 ns (17.6 %), step = 609.7 ps (203 m%) tran: time = 57.88 ns (22.6 %), step = 609.7 ps (203 m%) tran: time = 57.88 ns (22.6 %), step = 609.1 ps (203 m%) tran: time = 67.88 ns (22.6 %), step = 609.1 ps (203 m%) tran: time = 127.9 ns (32.6 %), step = 609.4 ps (203 m%) tran: time = 127.9 ns (42.6 %), step = 609.4 ps (203 m%) tran: time = 157.7 ns (52.6 %), step = 609.4 ps (203 m%) tran: time = 157.7 ns (52.6 %), step = 609.4 ps (203 m%) tran: time = 167.9 ns (62.6 %), step = 558.3 ps (106 m%) tran: time = 17.9 ns (62.6 %), step = 558.3 ps (106 m%) tran: time = 17.7 ns (72.6 %), step = 609.4 ps (203 m%) tran: time = 107.9 ns (62.6 %), step = 558.3 ps (106 m%) tran: time = 203.1 ns (67.7 %), step = 610.3 ps (270 m%) tran: time = 22.8 ns (77.6 %), step = 558.3 ps (106 m%) tran: time = 22.8 ns (77.6 %), step = 558.3 ps (106 m%) tran: time = 22.9 ns (97.6 %), step = 558.3 ps (206 m%) tran: time = 22.9 ns (97.6 %), step = 558.3 ps (206 m%) tran: time = 22.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: time = 22.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: time = 22.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: time = 22.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: time = 22.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: time = 22.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 22.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 20.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 20.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 20.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 20.9 ns (97.6 %), step = 609.2 ps (296 m%) tran: time = 20.9 ns (97.6 %), step = 609.4 ps (203 m%) tran: t | File Help | 6 |
| 17 | temp = 27 C trom = 27 C tempeffects = all errpreset = moderate method = traponly lteratic = 3.5 relref = sigglobal cmin = 0 F gmin = 1 pS marxed = 0 0hm mos_wres = 50 mV tran: time = 27.26 ms (7.52 %), step = 595 ps (198 m%) tran: time = 37.72 ns (12.6 %), step = 692.4 5 ps (200 m%) tran: time = 37.72 ns (12.6 %), step = 693.2 ps (298 m%) tran: time = 52.83 ns (17.6 %), step = 693.2 ps (298 m%) tran: time = 67.88 ns (22.6 %), step = 558.3 ps (186 m%) tran: time = 67.88 ns (22.6 %), step = 558.4 ps (200 m%) tran: time = 67.72 ns (32.6 %), step = 510.2 ps (298 m%) tran: time = 7.72 ns (32.6 %), step = 510.2 ps (298 m%) tran: time = 112.8 ns (37.6 %), step = 510.3 ps (270 m%) tran: time = 112.7 ns (42.6 %), step = 510.9 ps (203 m%) tran: time = 142.5 ns (47.5 %), step = 558.4 ps (186 m%) tran: time = 142.5 ns (47.5 %), step = 558.4 ps (186 m%) tran: time = 127.9 ns (62.6 %), step = 558.4 ps (186 m%) tran: time = 122.8 ns (57.6 %), step = 558.4 ps (186 m%) tran: time = 122.8 ns (57.6 %), step = 558.4 ps (186 m%) tran: time = 217.7 ns (22.6 %), step = 558.4 ps (186 m%) tran: time = 222.8 ns (77.6 %), step = 558.4 ps (186 m%) tran: time = 247.9 ns (62.6 %), step = 558.4 ps (186 m%) tran: time = 247.9 ns (62.6 %), step = 558.4 ps (186 m%) tran: time = 247.9 ns (92.6 %), step = 609.4 ps (203 m%) tran: time = 22.8 ns (77.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (77.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (77.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 ps (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 s (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 s (203 m%) tran: time = 22.8 ns (97.6 %), step = 610.9 s (203 m%) tran: time = 202.8 ns (9 | |

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Figure 7.7: Spectre log window for the NAND simulation



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Figure 7.9: Waveform output window in strip mode



Figure 7.10: Waveform output window: zoomed view



Figure 7.11: Waveform output with markers

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|-----------|----------|--------------------|-----|--|
| Library I | lame | tutorial | _ | |
| Cell Nam | e | nand-test | | |
| View Name | | confid | | |
| Tool | | Hierarchy-Editor 🖃 | | |
| Library p | ath file | | | |

Figure 7.12: Create New File dialog for the config view

| Top Cell Library: test | | Cell: | nand2_test | View: | schematic | Browse |
|---|--|---|--------------------------------------|-----------------------|-----------|--------|
| -Global Bindir | ngs | | | | | |
| Library List: | myLib | | | | | |
| View List: | spectre cr | nos_sch | cmos.sch schem | atic veriloga ah | dl | |
| Stop List: | spectre | | | | | |
| Description | | | | | | |
| Default templ Note: Please rer fields with | ate for spe nember to the actual | ctre replace ⁻ names u | Fop Cell Library, sed by your des | Cell, and View gn. | | |
| | OF | (c | ancel Use | Template | Help | |

Figure 7.13: New Configuration dialog box

| 🗧 Cadence® hie | erarc | hy editor: New Configu | uration (Save Needed) | | |
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| Ton Cell | | | | | |
| | | | | | |
| Library: test | | Cell: | nand2_test | View: schematic | Open |
| Global Bindin | gs | | | | |
| Library List: | mvL | ib | | | |
| | | | | | |
| View List: | spe | ctre cmos_sch cmos.s | ch schematic veriloga ahdl | | |
| Stop List: | spe | ctre | | | |
| Call Pindings | | | | | |
| Library | - | Call | View Found | View to Use | Inhoritod View List |
| NCSU Analog F | Pa | ran | spectre | VIEW CO USE | spectre cmos sch cmo |
| NCSU Analog F | Pa | nmos | spectre | - | spectre cmos sch cmo |
| NCSU Analog F | Pa | nmos | spectre | - | spectre cmos sch cmo |
| NCSU Analog F | Pa | res | spectre | | spectre cmos sch cmo |
| NCSU Analog F | Pa | vdc | spectre | | spectre cmos sch cmo |
| NCSU Analog F | Pa | voulse | spectre | | spectre cmos sch cmo |
| UofU Example | | nand2 | cmos sch | | spectre cmos sch cmo |
| test | | nand2 test | schematic | | spectre cmos sch cmo |
| Messages | varial | DIG 2421 FW_CD2_TIR | DIR at line number 1 | | |
| of file /uus FMP: Unset \$ v of file /uus Created new c | oc/fa /arial oc/fa | acility/cad_common/P ble SYSTEM_CDS_LIB_ acility/cad_common/P guration. | ICSU/CDK-F07/cdssetup/cds DIR at line number 1 ICSU/CDK-F07/cdssetup/cds | .lib .lib | |
| łeadv | | | | F | ilters OFE NameSnace: CDBA |

Figure 7.14: Hierarchy Editor view for nand-test (table view)

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| Top Cell | | | | | |
| Library: test | t Cell: nand2_test | View: schematic | Open | | |
| Global Bindii | ngs | | | | |
| Library List: | myLib | | | | |
| View List: | spectre cmos_sch cmos.sch schematic veriloga | ahdi | | | |
| Stop List: | spectre | | | | |
| Tree View | | | | | |
| | Instance | View to Use | Inherited View List | | |
| 🔺 (test nand2 | 2_test schematic) | | | | |
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| V2 (NCSU_Analog_Parts vdc spectre) spectre cmos_sch cmos.sch | | | | | |
| Messages | | | | | |
| of file /uu: | soc/tacility/cad_common/NCSU/CDK-F07/cdsset | up/cds.lib | | | |
| FMP: Unset \$ | variable SYSTEM_CDS_LIB_DIR at line number 1 | | | | |
| of file /uu: | soc/facility/cad_common/NCSU/CDK-F07/cdsset | up/cds.lib | | | |
| Created new | configuration. | | | | |
| Isaved the cur | rent coninguration to (test hand2_test config). | | • | | |
| Ready | | | Filters OFF NameSpace: CDBA | | |

Figure 7.15: Hierarchy Editor view for nand-test (tree view)



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| 🙀 Cadence® hi | erarchy editor: (test nand2_mixed config) | | |
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| File Edit V | iew | | Plug-Ins Help |
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| Top Cell | | | |
| Library: test | Cell: nand2_mixed | View: schematic | Open |
| -Global Bindii | ngs | | |
| Library List: | myLib | | |
| View List: | \$default | | |
| Stop List: | spectre spice verilog verilogNetlist | | |
| -Tree View | | | |
| | Instance | View to Use | Inherited View List |
| 🔺 (test nand2 | _mixed schematic) | | |
| 🛛 🛏 🗋 10 (Uofl | J_Example nand2 behavioral) | | \$default |
| 📙 🦰 I (Uofl | J_Example inv behavioral) | | \$default |
| 📙 🗋 12 (Uofl | J_Example inv behavioral) | | \$default |
| - 🖹 13 (Uofl | J_Example inv behavioral) | | \$default |
| - 🖹 14 (Uofl | J_Example inv behavioral) | | \$default |
| - 15 (Uofl | J_Example inv behavioral) | | \$default |
| - 16 (UofL | J Example inv behavioral) | | \$default |
| | 5U_Analog_Parts vdc spectre) | | \$default |
| | | | |
| | | | |
| Messages | | | |
| of file /uu: | soc/facility/cad_common/NCSU/CDK-F07/cdssetu | p/cds.lib | • |
| FMP: Unset \$ | variable SYSTEM_CDS_LIB_DIR at line number 1 | n (anta tila | |
| Created new | socyraciinty/cad_common/NCSU/CDK-FU//cdssetu configuration | p/cus.lib | 522 |
| Saved the cur | rent configuration to (test nand2_mixed config). | | ▼ |
| Ready | | | Filters OFE NameSpace: CDBA |

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Figure 7.17: Mixed-mode config view for mixed-nand

| X IE Defa | ault Option | 5 | | |
|------------------------|-------------|----------|-----------------|------|
| ок | Cancel | Defaults | Apply | Help |
| Default I | E Library | Name N | SU_Analog_Parts | |
| Default IE Model Name | | ame M | ĴŠ | |
| Detailed IE Generation | | tion _ | | |

Figure 7.18: Interface library dialog box

| XIE Model P | ropert | y Editor: (LII | BRARY `ti | utorial') |
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| ок с | Cancel | Defaults | Apply | Help |
| IE Library N | ame | NCSU_Ana | alog_Par | tsj |
| IE Model Na | me | MOŠ | | |
| Model 10 | | output = | | |
| | | | | Model Parameters |
| d2a_tf (defa | ault) | 2 rį | | |
| d2a_tr (defa | d2a_tr (default) | | | |
| d2a_vh (def | iault) | S | | |
| d2a_vl (defa | ault) | <u>ď</u> | | |
| macro (defe | udt) | | | |

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Figure 7.19: d2a interface element parameters

| 121 |
|-----|
|-----|

| X IE Mod | el Propert | y Editor: (LII | BRARY `tu | torial') |
|------------|------------|----------------|-----------|------------------|
| ок | Cancel | Defaults | Apply | Help |
| IE Library | / Name | NCSU_Ana | alog_Part | ्रम् |
| IE Model | Name | MOŠ | | |
| Model 10 | | input 🖃 | | |
| | | | | Model Parameters |
| a2d_tx (d | lefault) | 1mž | | |
| a2d_v0 (| default) | 1.5 | | |
| a2d_v1 (| default) | 3.5 | | |
| macro (il | efædt) | | | |

Figure 7.20: a2d interface element parameters

| 🐺 Cadence® hi | erarchy editor: (test nand2_mixed config) | | |
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| File Edit V | iew | | Plug-Ins Help |
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| Top Cell | | | |
| Library: test | Cell: nand2_mixed | View: schemati | c Open |
| -Global Bindir | ngs | | |
| Library List: | myLib | | |
| View List: | \$default | | |
| Stop List: | spectre spice verilog verilogNetlist | | |
| -Tree View- | | | |
| | Instance | View to Use | Inherited View List |
| 🔺 (test nand2 | 2_mixed schematic) | | |
| 🛉 🕂 🗂 10 (Uof L | J_Example nand2 analog_extracted) | analog_extracted | spectre |
| 🗣 🗂 I 1 (Uof L | J_Example inv cmos_sch) | cmos_sch | spectre |
| - 12 (UofL | J_Example inv behavioral) | | \$default |
| - 13 (UofL | J_Example inv behavioral) | | \$default |
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| • 115 (Unft | I Example invictions sch) | cmos sch | spectre |
| | I Example inv behavioral) | cirios_scii | \$default |
| | 5U_Analog_Parts vdc spectre) | | \$default |
| -Messages [Set view list to | ir instance "15" in cellview (test nand2_mixed sch | ematic) to "spectre". | |
| Saved the cur | rent configuration. | | |
| Bound instanc | e "IO" in cellview (test nand2_mixed schematic) t | o view "analog_extracted". | |
| Saved the cur | rent configuration. | ematic) to "spectre". | |
| Ready | | | Filters OFF NameSpace: CDBA |

Figure 7.21: Mixed-mode config view with analog/Verilog partitioning

| X Virte | uoso® Scl | hema | atic I | Editing | : test n | and2_m | iixed scl | hematic C | onfig: tesl | t nand2_n | nixed conf | ìg | | | | |
|----------------|-----------|------|--------|----------|----------|--------|-----------|----------------------|-------------|----------------|------------|--------------|----------|--------------|--------|-----|
| Cmo | 1: | | Se | l: 1 | | | | 0.1 | | | | | | | | 25 |
| 10015 | Design | Win | aow | Ealt | Add | Спеск | Sneet | Options | Migrate | Hierarch | y-Ealtor | Mixed-Signal | NCSU | | | нер |
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| € ² | | | | | | | | | | | | | | | | |
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| G | mouse L | : sh | IOWC. | lickIr | nfo() | | | M | : schHiM | ousePopU | þ() | | R: mspl | DisplayAllAc | tive() | |
| ~= | -> | | | | | | | | | • | - | | • | | | - |

Figure 7.22: The mixed-test schematic showing analog/digital partitioning

```
// Verimix stimulus file.
// Default verimix stimulus.
initial
begin
   a = 1'b0;
b = 1'b0;
#10 $display("ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $display("Error - that's wrong!");
a=1;
#10 $display("ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $display("Error - that's wrong!");
b=1;
#10 $display("ab = %b%b, out = %b", a, b, dout);
if (dout != 0) $display("Error - that's wrong!");
a=0;
#10 $display("ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $display("Error - that's wrong!");
end
```

Figure 7.23: The digital testbench for the mixed-nand simulation







Figure 7.25: Rearranged results of the mixed-mode simulation

```
Switching from DC to transient.
VERILOG time 0 (units of 100ps) corresponds to spectre time 0.
Message! At the end of DC initialization the logic values
         of the following ports are X (unknown):
          net16
          net18
                                                           [Mixed_Sig]
         "IE.verimix", 4: ...
ab = 00, out = 1
ab = 10, out = 1
ab = 11, out = 0
ab = 01, out = 1
Verilog/spectre Interface: 165 messages sent, 167 messages received.
0 simulation events
(use +profile or +listcounts option to count) + 29 accelerated events
CPU time: 0.0 secs to compile + 0.0 secs to link + 3.6 secs in simulation
End of Tool:
               VERILOG-XL
                               05.81.001-p Aug 23, 2006 10:58:39
```

Figure 7.26: \$display output from the mixed-test simulation

```
// Verimix stimulus file.
// Default verimix stimulus.
integer file; // declare the file descriptor first
initial
begin
  file = $fopen("/home/elb/IC_CAD/cadencetest/testout.txt");
   a = 1'b0;
  b = 1'b0;
$fdisplay(file, "Starting mixed-test simulation of NAND");
$fdisplay(file, "using digital inputs to an analog simulation");
#10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $fdisplay(file, "Error - that's wrong!");
a=1;
#10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $fdisplay(file, "Error - that's wrong!");
b=1;
#10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
if (dout != 0) $fdisplay(file, "Error - that's wrong!");
a=0;
#10 $fdisplay(file, "ab = %b%b, out = %b", a, b, dout);
if (dout != 1) $fdisplay(file, "Error - that's wrong!");
end
```

Starting mixed-test simulation of NAND
using digital inputs to an analog simulation
ab = 00, out = 1
ab = 10, out = 1
ab = 11, out = 0
ab = 01, out = 1

Figure 7.28: mixed-test testbench file with file I/O



Figure 7.29: Simple circuit for DC analysis (schematic view)

| OK Ca | ancel | Help |
|-------|---------|-------------------------|
| type | srcType | "Source type" |
| dc | vdc | "DC voltage" |
| mag | acm | "AC magnitude" |
| phase | acp | "AC phase" |
| tc1 | tc1 | "Temperature coefficier |
| tc2 | tc2 | "Temperature coefficier |
| tnom | tnom | "Nominal temperature" |
| | | |
| | | |

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| UK | Cancel | Defaults | Apply Choosin | ig Analyses Virt | uoso® Analog D |
|----------------|--|---|--|--|----------------------------------|
| Analy | /sis | tran xf pz pac qpss qpsp | ♦ dc > sens > sp > pnoise > qpac | ◇ ac ◇ dcmatch ◇ envlp ◇ pxf ◇ qpnoise | ◇ noise > stb > pss > psp > qpxf |
| Save Swe | 9 DC Ope ep Variak | erating Poir | DC Analysis nt 🗌 | | |
| | Tempera Design V Compone | ture ariable nt Parame | Compo iter Param | nent Name Select Com eter Name | /v1] ponent dď |
| Sweet Sweet | Tempera Design V. Compone Model Pa ep Range Start-Sto Center-S ep Type comatic | ture ariable nt Parame rameter 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 | Compo eter Param | select Com Select Com eter Name | /v1] ponent dcġ Šġ |
| Swee Add | Tempera Design V: Compone Model Pa ep Range Start-Sto Center-S ep Type comatic | ture ariable Int Parame rameter 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 | Compo Iter Param | select Com eter Name | /v1] ponent dđ |

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Figure 7.31: DC analysis dialog box

| 💥 ¥irtuoso® Analog Design E | nvironment (5) | |
|--------------------------------|--|--|
| Status: Selecting outputs | to be plotted T=27 C Simulator: spectre | 33 |
| Session Setup Analyses | Variables Outputs Simulation Results Tools | Help |
| Design | Analyses | Ł |
| Library test | # Type Arguments Enable | ⊐ AC © TRAN |
| Cell DC-test View schematic | 1 dc 0 5 Auto Star yes | |
| Design Variables | Outputs | ₽ |
| # Name Value | # Name/Signal/Expr Value Plot Save March | 4 |
| | 1 MO/D yes no no | ₹ • • • • • • • • • • • • • |
| > Select on Schematic Outp | Plotting mode: Replace = | |

Figure 7.32: Analog Environment dialog box for DC analysis

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| XParametric Analysis - spectre(6): test Tool Sweep Setup Analysis | DC-test schema | tic | | | Help 38 |
|--|--------------------------------------|----------|----|-------------------|----------|
| Sweep 1 Range Type Step Control | Variable Name From Total Steps | fog 1 | То | Add Specification | Select 📃 |

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Figure 7.34: Dialog to set variable parameters for parametric simulation



Figure 7.35: Output of parametric DC simulation with five curves



Figure 7.36: Test schematic for power measurements of a NAND gate



Figure 7.37: Analog simulation output from NAND gate simulation using Spectre



Figure 7.38: Waveform output with current plotted for the NAND simulation

| 🗙 Calculato | e . | | | | | | | | | | | _ 0 |
|-------------|---------|-------|----------|---------|----------|-----|------|--------|-------|----------|----------|------|
| Window M | lemorie | s Con | stants | Options | | | | | | | Hei | lp 4 |
| | | | | | | | | | | | | |
| Evaluate B | uffer | Di | isplay S | tack _ | 1 | | 🔶 st | andard | ⇔ RF | 8 | | |
| browser | vt | it | lastx | x<>y | dwn | up | sto | rcl | Spe | ecial Fu | inctions | - |
| wave | vf | ir | cle | ar | cist | app | sin | asin | mag | In | exp | abs |
| family | VS | is | en | ter | undo eex | eex | COS | acos | phase | log10 | 10**x | int |
| erplot | vdc | idc | - | 7 | 8 | 9 | tan | atan | real | dB10 | y**x | 1/x |
| plot | op | opt | + | 4 | 5 | 6 | sinh | asinh | imag | dB20 | x**2 | sqrt |
| printvs | vn | var | | 1 | 2 | 3 | cosh | acosh | fl | f2 | f3 | f4 |
| print | mp | | 1 | 0 | | +1- | tanh | atanh | | | | |

Figure 7.39: Dialog box for the Spectre Analog Environment calculator