

Chapter **6**

Standard Cell Design Template

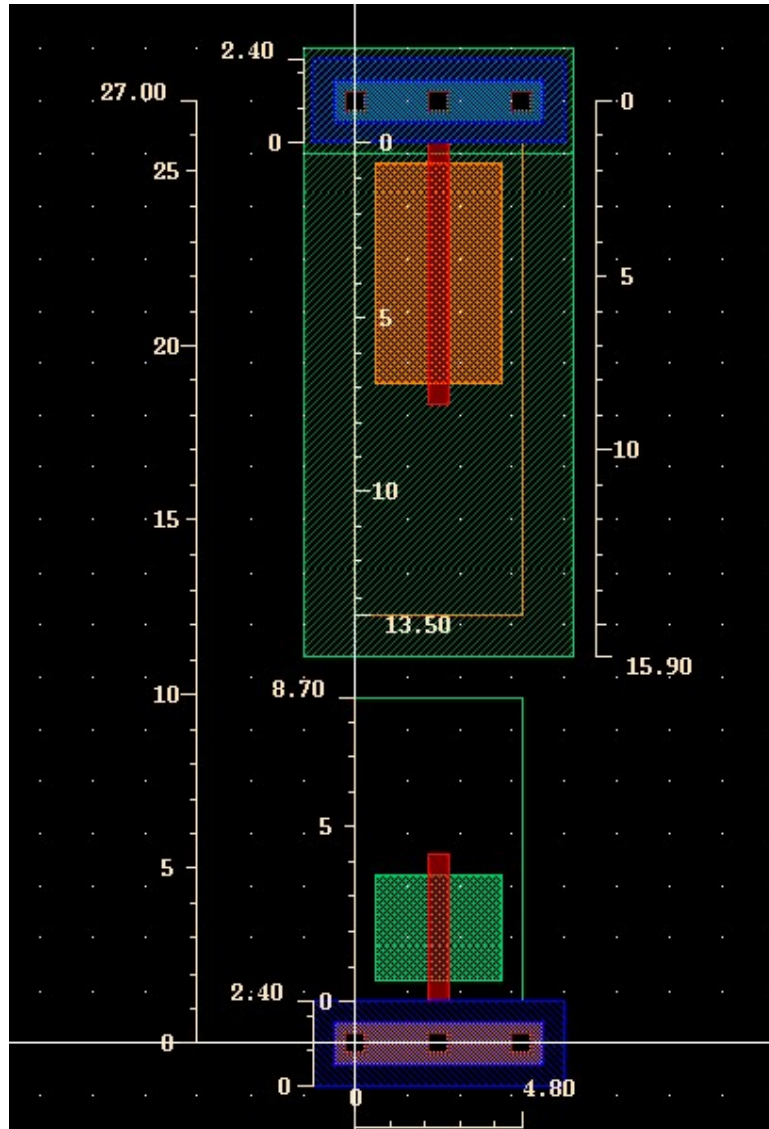


Figure 6.1: A layout template showing standard cell dimensions

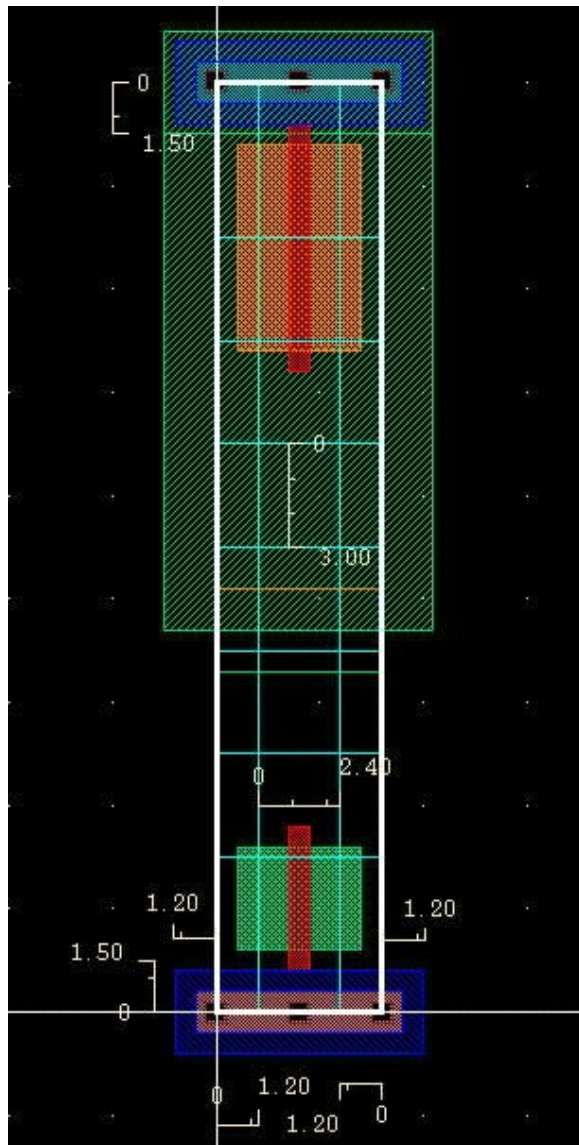
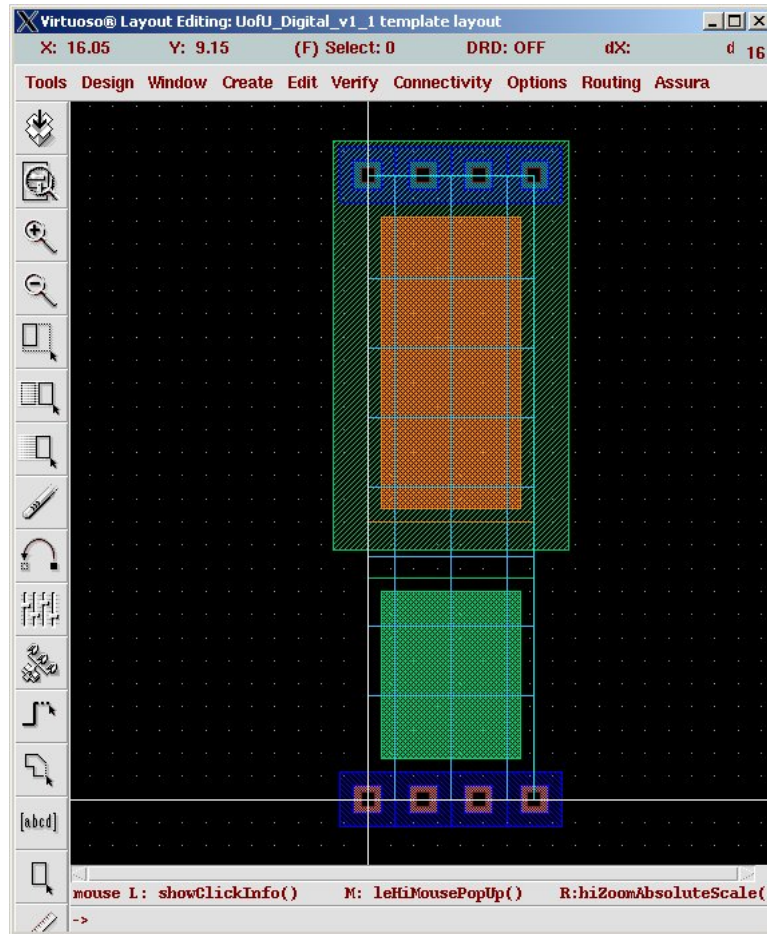
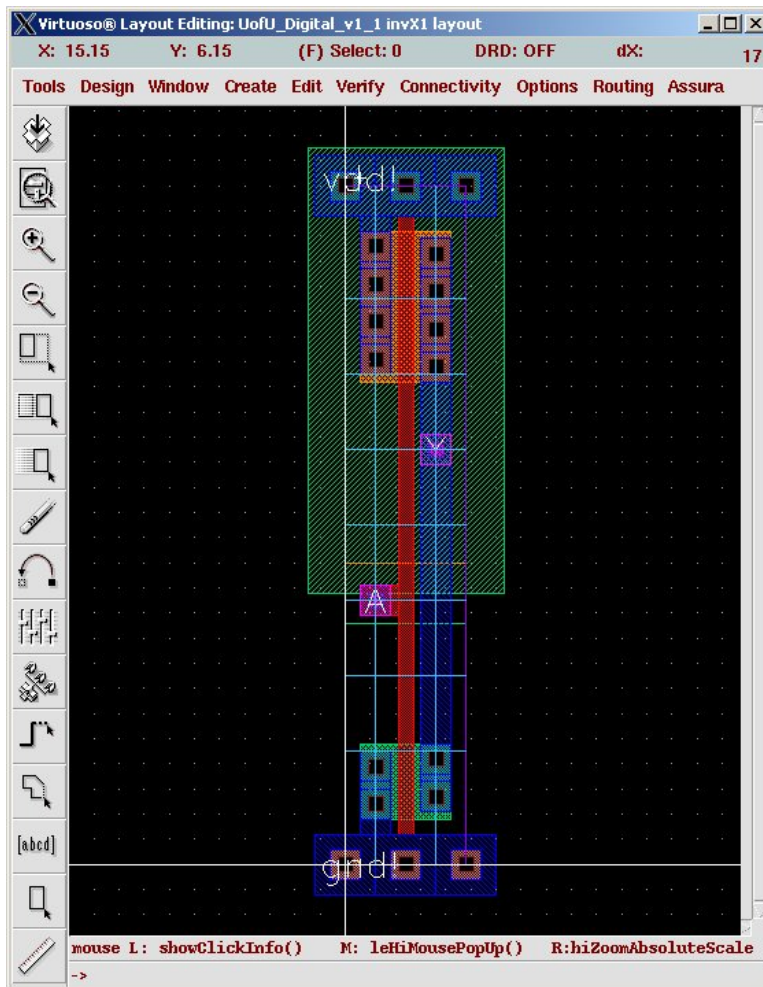


Figure 6.2: A layout template showing cell boundary (**prBound** layer)



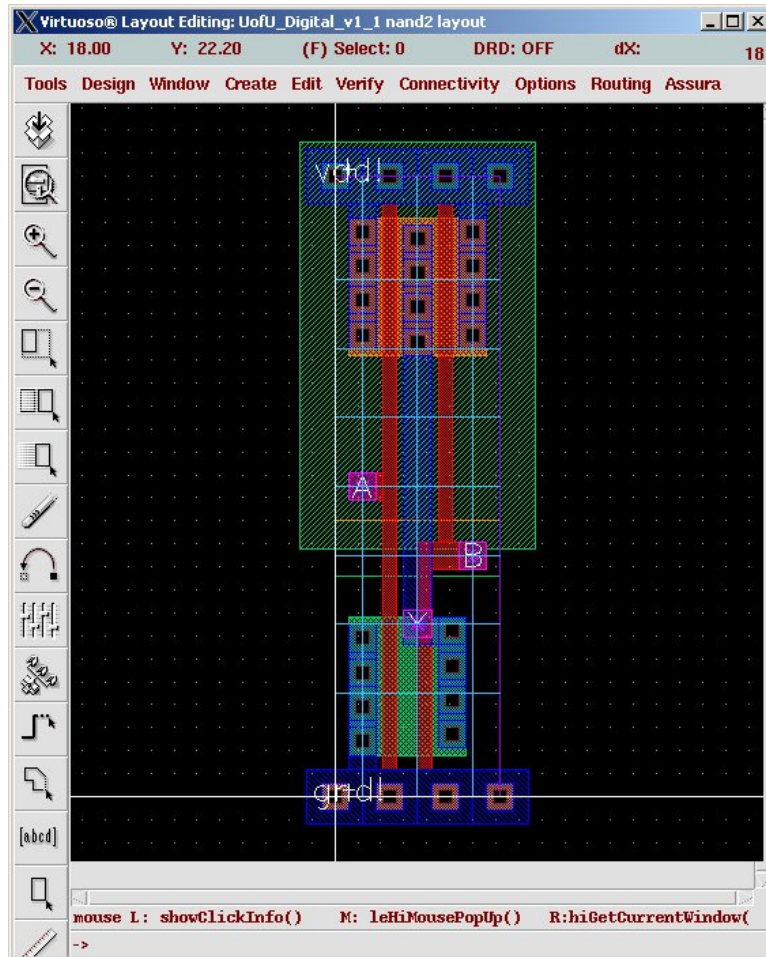
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Figure 6.3: A layout template for a four-wide cell



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Figure 6.4: Standard cell layout for a 1x inverter



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Figure 6.5: Standard cell layout for a 1x NAND gate