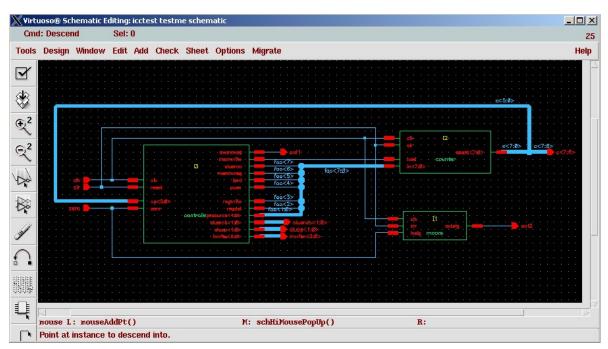
Chapter **12**

Chip Assembly



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Figure 12.1: Starting schematic showing the three connected modules

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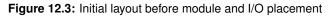
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Figure 12.2: The Gen From Source dialog box

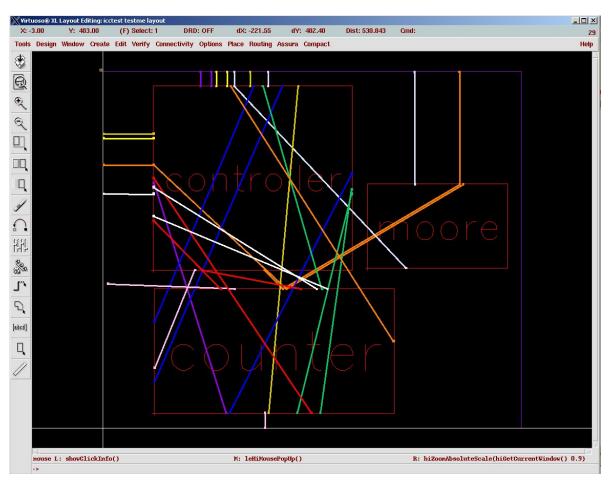
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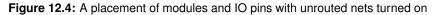
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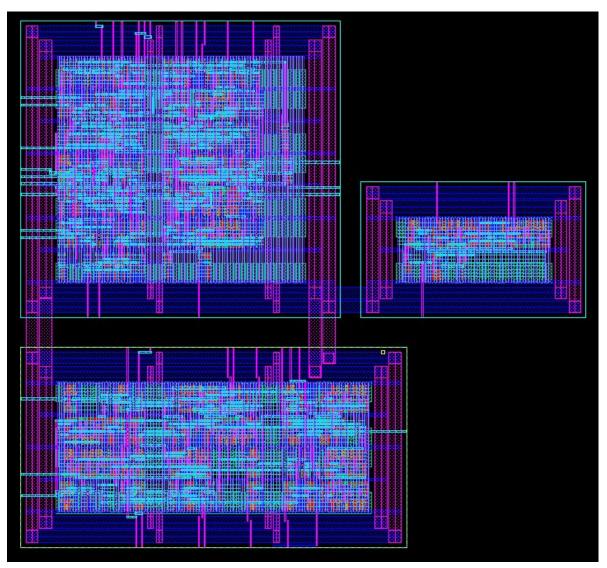


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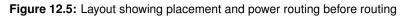


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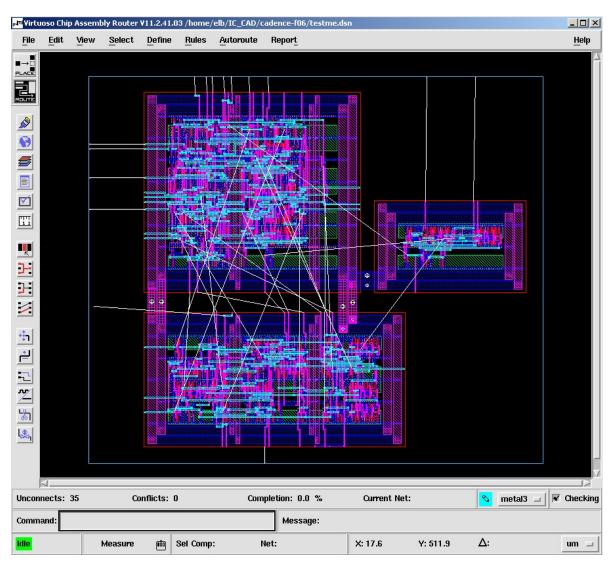


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Figure 12.6: Export to Router dialog box





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Figure 12.7: Initial ccar window

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Figure 12.8: Layer configuration dialog box

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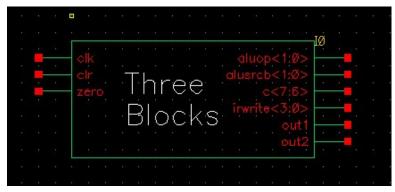
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Figure 12.9: Routing cost factor dialog box



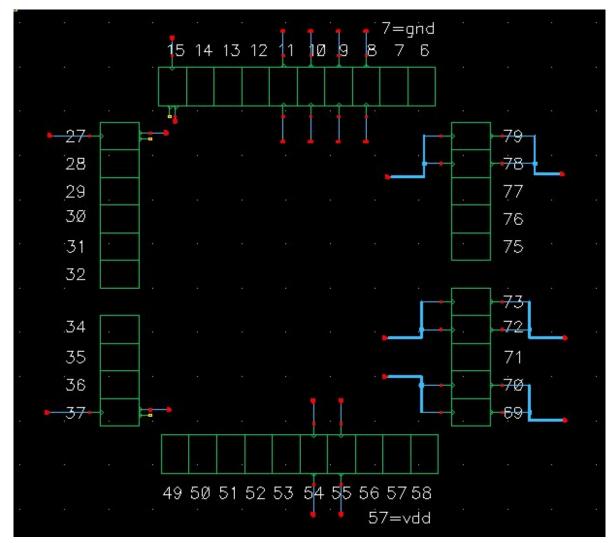
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Figure 12.10: Final routed circuit (shown in Virtuoso window)



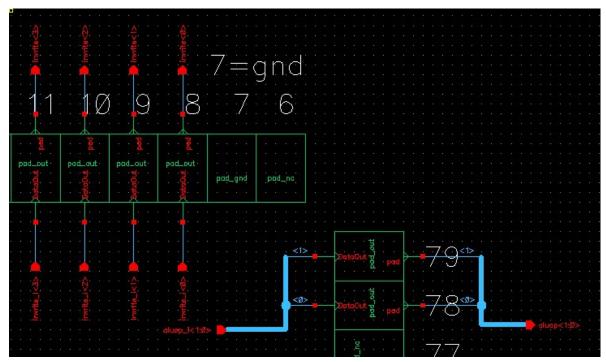
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Figure 12.11: Symbol for the Three Blocks example core



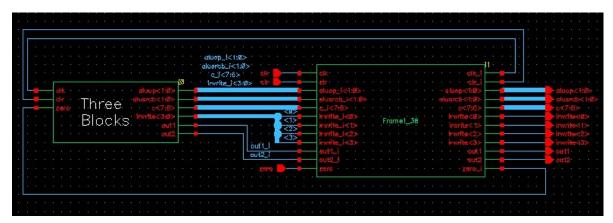
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Figure 12.12: Pad frame with signal wires



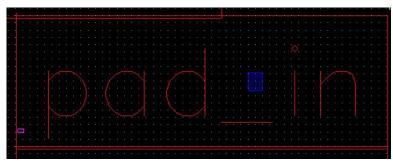
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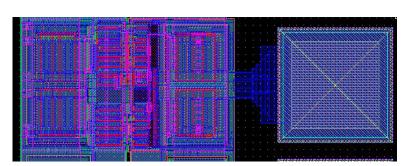
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Figure 12.14: Frame and core components connected together



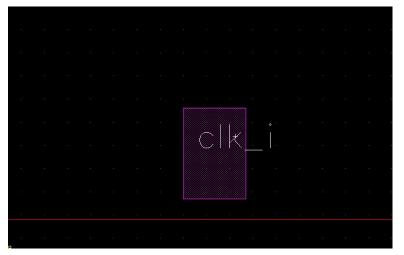
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Figure 12.15: pad_in cell with clk and clk_i connections



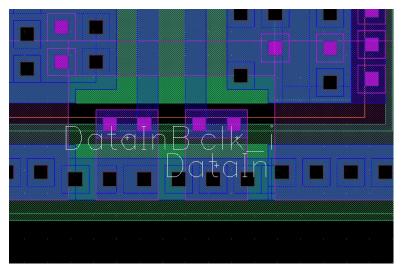
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Figure 12.16: Expanded pad_in cell with clk and clk_i connections



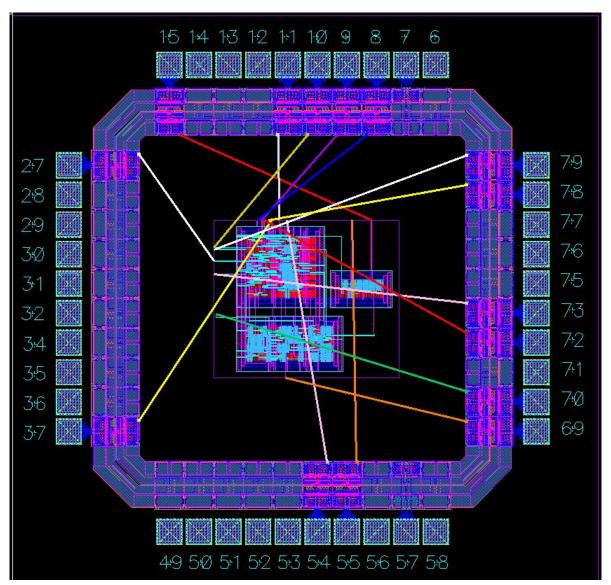
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Figure 12.17: Detail of clk_i connection



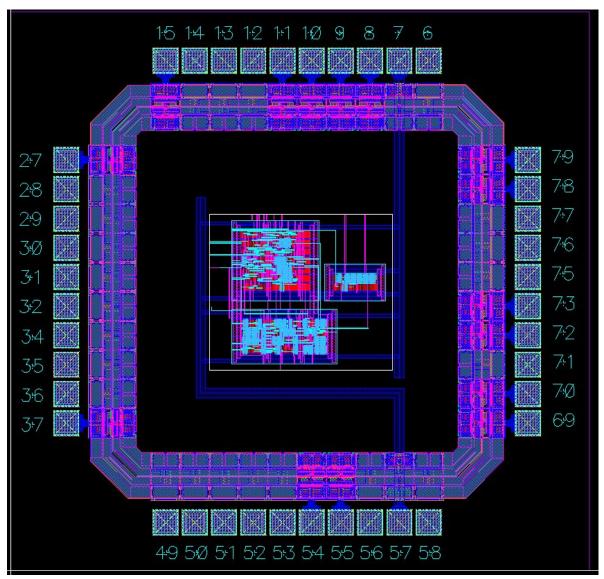
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Figure 12.18: Expanded detail of clk_i connection



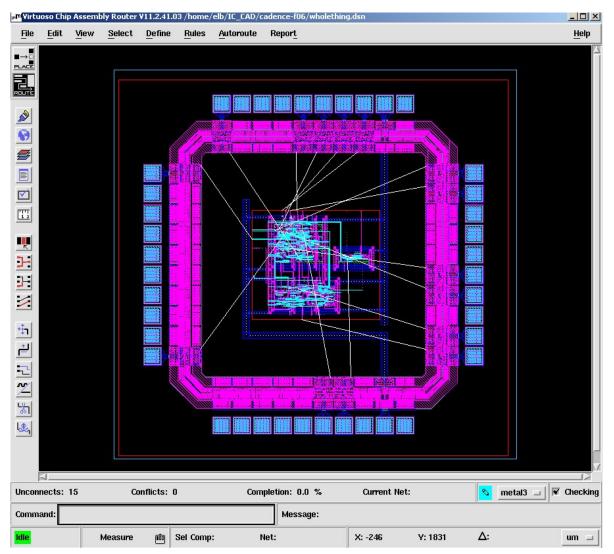
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Figure 12.19: Frame and core placed in Virtuoso-XL



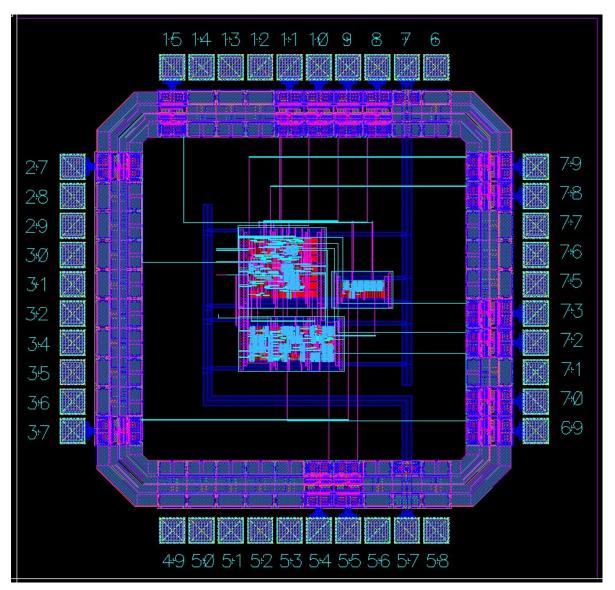
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Figure 12.20: Frame and core placed in *Virtuoso-XL* with vdd and gnd routing completed



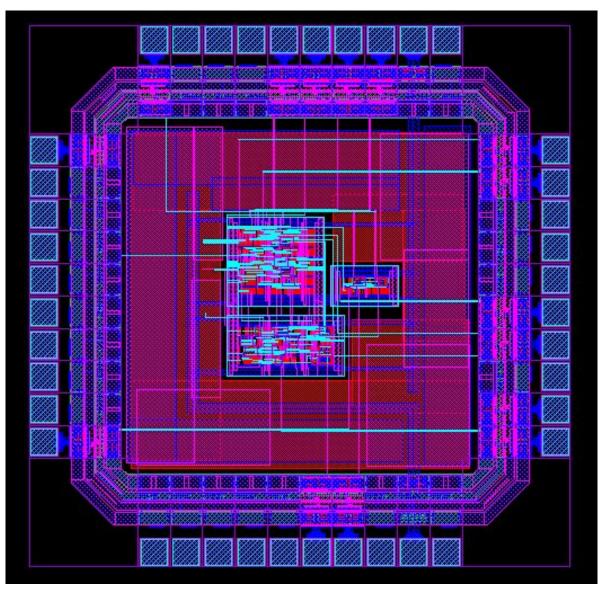
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Figure 12.21: Frame and core before routing in ccar



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Figure 12.22: Frame and core after routing in Virtuoso



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Figure 12.23: Final wholechip chip with extra rectangles of poly, metal1, and metal2 to meet minimum density requirements

Layer map for converting from cadence to GDS format # (SCMOS SCN3M SUBM processes through MOSIS) # Some of these layers are unlikely to be used.. . # Erik Brunvand, University of Utah # # Cadence layer Cadence layer purpose GDSII layer _____ # -----_____ drawing 42 0 nwell pwell drawing 41 0 # note that all three active layers map to GDS layer 43 active drawing nactive drawing 43 0 43 0 pactive drawing drawing 43 0 45 0 nselect drawing 44 0 pselect drawing poly 46 0 poly pin 46 0 drawing drawing 56 0 49 0 elec metal1 metal1 drawing metall pin metal2 drawing metal2 pin metal3 drawing metal3 pin # All four 49 0 51 0 51 0 62 0 62 0 # All four contact types go to GDS layer 25 2.5 0 cc drawing drawing 25 0 ca 25 0 ср drawing drawing drawing drawing drawing drawing drawing 25 0 50 0 ce via via2 61 0 qlass 52 0 pad highres res_id 26 0 drawing 34 0 34 0 drawing

Figure 12.24: GDSII map file for SCMOS circuits fabricated through AMI on their C5N CMOS process

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Figure 12.25: Initial Export Stream dialog box

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Figure 12.26: User-Defined Data dialog box for Export Stream



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Figure 12.27: Completion indication from the Export Stream process

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Figure 12.28: Map file for importing GDSII into DFII